ISCAS ’98

1998 IEEE International Symposium on Circuits and Systems

May 31 - June 3, 1998
Monterey Conference Center
Monterey, CA

Final Program

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Welcome to ISCAS' 98 and Monterey

On behalf of the Organizing Committee, it is our pleasure to invite and welcome you to the 1998 IEEE International Symposium on Circuit and Systems (ISCAS'98), to be held in the beautiful and historic city of Monterey, California. The 1998 ISCAS, sponsored by the IEEE Circuits and Systems Society and hosted by the Naval Postgraduate School of Monterey, CA, will be held at the Monterey Conference Center in conjunction with the Monterey Marriott and Doubletree Hotels, from May 31 through June 3, 1998.

The technical program this year consists of 97 sessions that cover a broad range of technical subjects. Among these are 16 Special Invited Sessions that have been organized and selected to bring you the most current thinking and research results in the field. Two panel discussions on Education and Government sponsored research, along with three plenary presentations are also planned. In addition to the regular technical program, 13 specially organized short courses are scheduled on Sunday, May 31, preceding the start of the regular program.

A number of social events are planned throughout the conference, including a Welcoming Reception on Sunday evening, a conference reception and concert at the Naval Postgraduate School on Monday evening, and a Banquet at the Monterey Bay Aquarium on Tuesday evening. Additionally, spouse and dependent activities are also organized which include a bus tour of Monterey, Pebble Beach, Carmel, Big Sur and a wine tasting tour to Carmel Valley.

The conference is an excellent opportunity for researchers to meet in a relaxing and stimulating environment. Apart from the beauty of its coastline, the Monterey Peninsula, situated in central California (2 hours south of San Francisco), is the habitat of a rich wildlife. Sea otters, sea lions and migrating whales can be seen in their natural settings.

The Monterey Conference Center with the Monterey Marriott and Doubletree Hotels, the venue of ISCAS'98, are located in downtown Monterey a few minutes walk from the Fisherman's Wharf and Cannery Row with their numerous restaurants, the beach and the main attractions of Monterey. Other close attractions like the 17 Mile Drive with its world famous Pebble Beach golf courses and Carmel-by-the-Sea with its European style boutiques, are within a short drive. They will conspire to pull you away from the Symposium,.but you will heroically resist.....most of the time.

We sincerely hope you enjoy your visit to Monterey, and you will remember both the technical and social aspects of ISCAS' 98 as a pleasant and worthwhile experience.

Sherif Michael
General Chairman
ISCAS '98

Stanley A. White
General Co-Chairman
ISCAS '98

Message from Technical Program Co-Chairs

On behalf of the Technical Program Committee, it is our pleasure to introduce the Technical Program for ISCAS'98. This program represents the integrated efforts of many individuals, namely, the authors, special session organizers, reviewers, and the Technical Program Committee. The entire review process was carried out on-line and a significant fraction of the papers were provided in publish ready Adobe Acrobat Portable Document Files (pdf).

We received over 1200 papers from various parts of the globe. In selecting papers, the Technical Program Committee had the excruciatingly difficult task of selecting among many papers of near equivalent quality. It is tempting to draw the conclusion that if a paper was not accepted, it must have been judged a poor or unqualified paper. Although there were such papers submitted, many of the papers that we could not fit into the ISCAS'98 technical program were fine papers.

The Technical Program is comprised of 779 contributed and 140 special session papers. There are three Plenary Talks, two Panel Discussions, 18 Special Sessions and 79 Regular Sessions. With the exception of the plenary session, there will be over 15 parallel sessions each morning or afternoon. About 43% of the papers will be presented in Poster Sessions which have the advantage of allowing attendees to meet the authors personally and to discuss their papers in depth. The Technical Program Committee made no quality differentiation in selecting papers for poster and oral sessions. Papers were assigned with the sole purpose of forming coherent sessions.

We would like to take this opportunity to thank all authors who submitted papers, the reviewers, the Track Chairs, the Members of Technical Program Committee, the Special Sessions Chair, and the special session organizers; they all have contributed mightily to the success of the Technical Program for ISCAS'98.

Kenneth R. Laker and Murali Tummala
Technical Program Co-Chairs
ISCAS '98

ISCAS '98 COMMITTEE CHAIRS

General Chair
Professor Sherif Michael
Naval Postgraduate School
gchair@iscas.nps.navy.mil

General Co-Chair
Dr. Stanley White
SPACE Corporation
cochair@iscas.nps.navy.mil

Technical Program Co-Chair
Professor Murali Tummala
Naval Postgraduate School
tchair@iscas.nps.navy.mil

Technical Program Co-Chair
Professor Kenneth Laker
University of Pennsylvania
k.laker@ieee.org

Special Sessions Chair
Professor W. Kenneth Jenkins
University of Illinois,
Urbana-Champaign
special@iscas.nps.navy.mil

Plenary Sessions Chair
Professor Herschel Loomis, Jr.
Naval Postgraduate School
plenary@iscas.nap.navy.mil

Publications Chair
Dr. Philip Lopresti
Independent Counsel
publish@iscas.nps.navy.mil

Publicity Chair
Professor Lawrence P. Huelsman
University of Arizona
publicity@iscas.nps.navy.mil

Electronic Media Chair
Professor John McEachen
Naval Postgraduate School
pubmedia@iscas.nps.navy.mil

Exhibits Chair
Professor Russ Duren
Naval Postgraduate School
exhibits@iscas.iscas.nps.navy.mil

Short Courses Co-Chair
Professor Wasfy Mikhael
University of Central Florida
wbm@ece.engr.ucf.edu

Short Courses Co-Chair
Professor Philip Pace
Naval Postgraduate School
shcource@iscas.nps.navy.mil

Finance Chair
Professor David Jenn
Naval postgraduate School
finance@iscas.nps.navy.mil

Registration Co-Chairs
Professor John Ciezki and
Professor Robert Ashton
Naval Postgraduate School
register@iscas.nps.navy.mil

Local Arrangements Chair
Professor Todd Weatherford
Naval Postgraduate School
arrange@iscas.nps.navy.mil

ISCAS Steering Committee Chair
Professor Hari C. Reddy
California State University, Long Beach
hreddy@engr.csulb.edu

International Coordinators

Europe Chair
Professor George Moschytz
Swiss Federal Institute of Technology
moschytz@isi.eee.ethz.ch

South and Central America Chair
Professor Paulo Diniz
University Fed do Rio de Janeiro
diniz@coe.ufrj.br

Far East Chair
Professor Yong Ching Lim
National University of Singapore
elelimyc@leonis.nus.sg

Conference Schedule at a Glance

Saturday, May 30, 1998

6:00 PM – 9:00 PM ……Tutorial Registration and Reception…….....Portola Lobby

9:00 AM - 12:00 PM ……..Tutorial Morning Session.....….....(See Room Schedule – page 28)

1:00 PM - 5:00 PM ……Tutorial Afternoon Session.....(See Room Schedule – page 28)

6:00 PM - 9:00 PM ……Presymposium Reception.....DeAnza Ballroom

Exhibitors of ISCAS '98 will host the Presymposium Reception at the Monterey Conference Center.

Monday, June 1, 1998

7:30 AM – 5:30 PM ……Conference Registration.....Portola Lobby

8:00 AM ……...Opening of Conference.....Serra Grand Ballroom

8:05 AM - 8:45 AM ……..Keynote Speaker.....Serra Grand Ballroom

Mr. Jack Harding - President and CEO, Cadence Design Systems, Inc.
Title: System-On-A-Chip and the Path to Design Realization

9:00 AM – 12:30 PM ……Morning Technical Sessions.....(See Room Schedule – page 28)

2:00 PM – 5:30 PM ……Afternoon Technical Sessions.....(See Room Schedule – page28)

6:00 PM - 9:45 PM ……Award and Social Reception.....Naval Postgraduate School

*6:00 PM - 745 PM - **Social Reception**, the Barbara McNitt Ballroom at the Naval Postgraduate School*
*8:00 PM - 8:35 PM - **Awards Ceremony**, King Hall Auditorium at the Naval Postgraduate School*
8:30 PM - 8:40 PM - "A Farewell to Dr. Richard Hamming"
*8:45 PM - 9:45 PM - **Monterey Symphony Concert**, King Hall Auditorium, Naval Postgraduate School*

Tuesday, June 2, 1998

7:30 AM – 5:30 PM ……Conference Registration.....Portola Lobby

8:05 AM - 8:45 AM ……,,,……..Plenary Speaker.....Serra Grand Ballroom

Dr. Robert Trew - Department of Defense, Office of the Director, Defense Research and Engineering
Title: DoD Basic Research in Circuits and Systems

9:00 AM – 12:30 PM ……..Morning Technical Sessions.....(See Room Schedule – page 28)

2:00 PM –3:30 PM.……...Afternoon Technical Sessions....(See Room Schedule – page 28)

4:00 PM - 5:30 PM ……Panel Discussions

Panel Discussion Topics:
Government Research Funding (Serra Grand Ballroom)
Teaching Circuits, Systems, Electronics and Signal Processing in the 21st Century (Steinbeck Forum)

7:30 PM - 11:00 PM ……..Symposium Banquet at the Monterey Bay Aquarium

Monterey Aquarium, 1 Cannery Row, Monterey

*The symposium participants will be hosted by the world renowned **Monterey Aquarium** to a private party featuring a superb array of music, dining and of course sea creatures.*

Wednesday, June 3, 1998

7:30 AM – 5:30 PM ……Conference Registration.....Portola Lobby

8:05 AM - 8:45 AM ……..Plenary Speaker.....Serra Grand Ballroom

Dr. Greg Papadopoulos, Vice President, Chief Technology Officer, Sun Microsystems, Inc.
Title: Billions and Billions of Devices Served: Fundamental Challenges for the Network Age

9:00 AM – 12:30 PM ……Morning Technical Sessions.....(See Room Schedule – page 28)

2:00 PM – 5:30 PM ……..Afternoon Technical Sessions.....(See Room Schedule – page 28)

End of Conference

Special Invited Talks and Panels

Plenary Monday

8:05am – 8:45am – Serra Ballroom

Mr. Jack Harding - President and CEO, Cadence Design Systems, Inc.
Title: System-On-A-Chip and the Path to Design Realization

Mr. Harding was appointed as President and CEO of Cadence in October 1997. He joined Cadence in May 1997 as Senior Vice President of Cadence's Strategic Business Group. Prior to joining the company, he was President and CEO of Cooper & Chyan Technology (CCT) since December 1994 until it was acquired by Cadence in May 1997. other firms where he served include Zycas Corporation, TXL Corporation and IBM. Mr. Harding serves as a member of the Council on Competitiveness in Washington, DC, a non-partisan organization of chief executives from industry and academia working to advance U.S. global competitiveness. In addition, Mr. Harding serves on the Council's Executive Committee.
Mr. Harding received a BA in Chemistry and Economics from Drew University, where he is a member of the Board of Trustees.

Plenary Tuesday

8:05am – 8:45am – Serra Ballroom

Dr. Robert Trew - Department of Defense, Office of the Director, Defense Research and Engineering
Title: DoD Basic Research in Circuits and Systems

Robert J. Trew serves as Director for Research, Office of the Director, Defense Research and Engineering in the Office of the Secretary of Defense. He is responsible for providing scientific leadership, management oversight, policy guidance and coordination of the $1.2 billion yearly basic research programs of the Military Services and Defense Agencies. In this capacity, Dr. Trew has cognizance over the complete spectrum of efforts in research including physics, materials, chemistry, biology, electrical engineering and electronics, computer engineering and science, mathematics, environmental sciences and aerospace. In addition, he is responsible for science, mathematics and engineering education, policy for grants, cooperative agreements and executing the University Research Initiatives and other research efforts administered by the Office of the Secretary of Defense.

Dr. Trew has extensive experience in industry, academia and government. Dr. Trew serves on the Administrative Committee of the microwave Theory and Techniques Society of the Institute of Electrical and Electronics Engineers. He was the Editor of the IEEE *Transactions on Microwave Theory and Techniques* from 1995 to 1997. He is a Fellow of the IEEE. From 1976 to 1993, he was on the faculty of North Carolina State University where he served as Professor of Electrical and Computer Engineering. From 1993 to 1997, he was Geroge S. Dively Professor of Engineering and Chair of the Department of Electrical Engineering and Applied Physics at Case Western Reserve University. He was a visiting Professor at the University of Duisburg in Germany in 1985. He has published more than 130 technical articles, 13 book chapters and given over 180 scientific and technical presentations.

Panel Discussion Sessions

I. Government Research Funding

4:00pm – 5:50 pm – Serra Grand Ballroom

A panel discussion will be held on the aspects of future direction of research funding. Various members from all of the major research funding organizations will present their understanding of their organization's direction and then the panel will discuss topics provided by the attendees.

II. Teaching Circuits, Systems, Electronics and Signal Processing in the 21st Century

4:00pm – 5:50 pm – Steinbeck Forum

Organized by: Art Davis (San Jose State University) and Ken Jenkins (University of Illinois)
Panel Chairman: Ken Jenkins
Participants: Art Davis, San Jose State University
David Munson, University of Illinois at Urbana-Champaign
Gary Ford, University of California, Davis
John Choma, University of Southern California
Yannis Tsividis, Columbia University
Paulo Diniz, Federal University of Rio de Janiero

In recent years, many universities have struggles with important questions concerning how the topics of circuits, systems electronics, and signal processing can be best taught within the context of new rapidly emerging technologies. There is a great deal of pressure to integrate new topics into the Electrical and Computer Engineering (ECE) curriculum, while continuing to teach the fundamentals of engineering science that will prepare students to deal with rapidly changing technologies throughout their entire careers. Many universities have substantially revised their ECE curricula in the last few years, adding courses on new topics, dropping old topics and rearranging the order in which certain traditional topics are taught. Some universities have initiated new efforts in outreach education, including off-campus degree programs offered by satellite and internet modalities, as well as non-degree continuing education programs aimed more at skill-sharpening for practicing engineers. The question to teaching "analog or digital first" is still widely debated, as are the related questions of what to include and what to exclude in an increasingly crowded ECE curriculum.

This panel will debate many of these important issues concerning the teaching of circuits, systems, electronics and signal processing in the 21st Century. Each panelist will open with a brief position statement, after which important issues will be debated. Audience participation is encouraged.

Plenary Wednesday

8:05am – 8:45am – Serra Ballroom

Dr. Greg Papadopoulos, Vice President, Chief Technology Officer, Sun Microsystems, Inc.
Title: Billions and Billions of Devices Served: Fundamental Challenges for the Network Age

As Chief Technology Officer for Sun Microsystems, Inc., Dr. Greg Papadopoulos is responsible for assessing Sun's technological investments, as well as directing the activities of Sun Laboratories and associated advanced

development programs. At Sun, Dr. Papadopoulos has held senior positions as Vice President of Technology and Advanced Development for SMCC, and Chief Scientist for Server Systems Engineering and then the Enterprise Servers and Storage business unit within SMCC.

Dr. Papadopoulos joined Sun in the fall of 1994 from Thinking Machines where he was Senior Architect and Director of Product Strategy and also an Associate Professor at MIT. At MIT, he conducted research in scalable systems and fault-tolerant computing. He was a development engineer at Hewlett-Packard and Honeywell and co-founded three companies: PictureTel, Ergo and Exa Corporation. Dr. Papadopoulos received a BA in systems science from UCSD and his MS and PhD in electrical engineering and computer science from MIT.

Receptions and Social Events

Presymposium Tutorial Reception

Saturday, May 30, 1998 …….. 6:00PM – 9:00PM
(DeAnza Ballroom)

Presymposium Reception

Sunday, May 31, 1998 …….. 6:00PM – 9:00PM
Exhibitors of ISCAS ’98 will host a Wine and Cheese Reception at the Monterey Conference Center.
(DeAnza Ballroom)

Award and Social Reception at the Naval Postgraduate School

Monday, June 1, 1998 …….. 6:00PM – 9:45PM

A social reception will be held Monday evening starting at 6:00PM, at the Barbara McNitt Ballroom in Hermann Hall on the Naval Postgraduate School (NPS) campus. The campus is located one mile east of the Monterey Conference Center. You can walk or take your car. A few buses will be available to and from NPS.

The reception will be held in the historic Del Monte Hotel (now named after Rear Adm. Ernest Edward Herrmann, first superintendent of NPS) build originally in 1881. The Del Monte was a famous resort owned by the railroad barons of the Southern Pacific and later by Samuel Morse’s nephew, until the U.S. Navy purchased the property in 1949 for the Postgraduate School. This ballroom has entertained such dignitaries as Greta Garbo, Johnny Weismuller, Presidents Ulysses S. Grant and Theodore Roosevelt.

A feast of Hors d’oeuvres, drinks and refreshments will be served until 7:45 PM. You will then follow the bagpiper who will lead you to King Hall Auditorium on the NPS campus, where the activities will continue with the Awards ceremony. At 8:45 PM, the Monterey Symphony Orchestra will provide a special concert until 9:45 PM. (All conference attendees are invited to this festive evening.)

The ISCAS’98 Banquet at the Monterey Bay Aquarium

Tuesday, June 2, 1998 …….. 7:30 PM – 11:00PM

The Monterey Bay Aquarium will host a special evening of wine, refreshments, music and appetizing food for ISCAS attendees. You can walk along the famous Cannery Row to the Aquarium or take your car. A few buses will be available to and from the aquarium.

The aquarium (www.mbayaq.org) is at the heart of the nation's largest marine sanctuary. More than a hundred galleries and exhibits re-create the bay's many habitats, from shallow tide pools to the vast open ocean. The exhibits include a million-gallon indoor ocean, viewed through the largest window on Earth, a towering three-story kelp forest, and jewel-box exhibits that reveal the delicate beauty of smaller sea creatures. You’ll be eye-to-eye with more than 350,000 strange and colorful creatures that live in the Monterey Bay, from playful sea otters and delicate jellies to powerful sharks, elusive octopus and giant ocean sunfish. You can stroke the rough skin of an

ochre star or the velvety back of a bat ray. You can also turn a telescope toward a sea otter in the kelp beds offshore or a microscope on dancing plankton. Videos, special programs and a host of hands-on activities bring the entire family closer to sea life than ever before. (A free ticket for this event is included with each full registration.) Extra tickets are available at the conference registration desk.

Organized Tours

Three tours are planned for the attendees of ISCAS 98 by Otter Tours & Charters. Room is available for 46 participants on each tour. Please note, if there are insufficient sign-ups for a particular tour, the tour may be canceled. So please enroll early so you don't miss on these well-valued tours.

Point Lobos/Big Sur Tour – Monday, 1 June 1998

Price: $50.00 per person before 11 May/ $60.00 after May 11

Make sure you bring your camera and film for this one. The tour departs 9:30 AM on Monday June 1, 1998, from the Doubletree Hotel. You will visit Point Lobos, the "Crowned Jewel of California's State Parks", what Francis McComas called the "Finest Meeting of Land and Water in the World". You'll enjoy a gentle nature walk learning the history, flora and fauna. Following Point Lobos, you'll continue down the scenic Pacific Coast Highway viewing some of the most spectacular views in North America. Once in famous Big Sur, you'll visit the world renowned Ventana Inn where you can have lunch while viewing breathtaking scenery. (Note: Lunch expense is not provided in Point Lobos/Big Sur tour cost). After lunch, you'll continue your tour of Big Sur shops and sites and return to the Doubletree by 3:00 PM.

Steinbeck/Wine Tasting Tour – Tuesday, 2 June 1998

Price: $65.00 per person before 11 May/ $75.00 after May 11

This will be a treat for your palate, a wine and food tour of what makes Monterey county world famous agriculturally. The tour departs 9:15 AM on Tuesday June 2, 1998, from the Doubletree Hotel. You will first visit the Chateau Julien Vineyards, where you may taste the fruits of their vines. The Monterey region is renowned for world-class varieties of Chardonnay and White Riesling. Following the Chateau Julien vineyard tour, you'll arrive for a private lunch at the Steinbeck House in Salinas. The childhood home of John Steinbeck is where he immortalized East of Eden in the center of Salinas Valley agriculture. Following the lunch, you'll arrive at Monterey Vineyards in Gonzales for more wine tasting (check out their Riesling). You'll return to the Doubletree by 3:30 PM.

Carmel/Monterey Shopping Tour – Wednesday, 3 June 1998

Price: $45.00 per person before 11 May/ $55.00 after May 11

Have your shopping shoes in shape! The tour departs at 9:00 AM on Wednesday June 3, 1998, from the Doubletree Hotel. You will tour the historic landmarks of the Peninsula. Your tour guide will show you the Indian burial grounds, adobes, early Monterey landmarks, Colton Hall, Robert Lewis Stevenson House, the Old Custom House, Fisherman's Wharf, Cannery Row, Pacific Grove, Asilomar, Pebble Beach's 17 Mile Drive, Carmel and the Carmel Mission. At noon, the tour bus will allow you to "shop 'til you drop" in the Carmel shopping district. Stop by Clint Eastwood's Hog's Breath Inn and "Make your day!" If you're still standing, the bus will return you at the Doubletree by 3:00 PM.

General Information

Location

Monterey (**www.monterey.com**) is located 100 miles south of San Francisco and 330 miles north of Los Angeles, on the southern edge of Monterey Bay. The locality is rich in history, wildlife and recreation. Since Commodore Sloat took the city without a shot in 1846 during the Mexican War, Monterey was the first capital of California until the Gold Rush of 1849. The quiet seaside resort became the center of the sardine industry in the early 1900's as brought to life by Steinbeck's novel *Cannery Row*. Today, the "Peninsula" has gone from making a living from the sea to being the foremost to protect sea life. The Monterey Bay Marine Preserve is home to countless marine animals, sea lions, otters, whales and dolphins. The Monterey Bay Aquarium, center of Monterey Bay Aquarium Institute (MBARI), provides young and old, hands-on and close up views of our aquatic friends. Early June should provide many photo opportunities of sea lions and otters along the coastline. Because of the natural beauty and rich habitat, thousands come to Monterey to enjoy many activities by the sea, such as scuba diving, sailing, salmon fishing, boating, ocean kayaking. Landlubbers can easily be kept occupied with golfing on 17 world class courses, biking along many of Monterey's bike trails, walking the white sand beaches of Carmel Bay, short jaunts at Point Lobos, Big Sur or Jack's Peak. Another popular sport on the Peninsula is shopping. All types of shop experiences

exist, from the outlet stores of Cannery Row to the unique European boutiques of Carmel. Finally, attendees will have multiple choices of some of the best restaurants in the world.

Getting to Monterey

Airlines

Two airlines and two car rental agencies will provide reduced rates to ISCAS ’98 attendees and their families. Discount fares are available for flight destinations by both carriers at:

1.) Monterey Peninsula Airport, 3 miles from conference,
2.) San Jose International Airport, 70 miles from conference,
3.) San Francisco International Airport, 100 miles from conference, and
4.) Oakland International Airport, 100 miles from conference.
Direct flights to Monterey exist between San Francisco and Los Angeles.

United Airlines

United Airlines is offering a 10% discount off the unrestricted mid-week coach fare or 5% discount off any published airfare from First Class to the lowest applicable discount to all attendees of the IEEE ISCAS ’98. United Airlines is also pleased to offer an additional 5% discount towards the purchase of tickets purchased at least 60 days in advance of travel. This special offer applies to travel on domestic segments of all United Airlines, United Express and Shuttle by United flights. United Airline's convenient schedule and discounted fares are available through their Meeting Desk. Call **1-800-521-4041** and reference Meeting ID Code **570IX**. Dedicated reservation personnel are on duty seven days a week from 7:00 AM to 12:00 Midnight EST.

Car rental discounts of 10% with Avis and Alamo car companies are offered through reservations with United. Please use meeting discount **#389817** and rate code **GR** with Alamo. For Avis, please refer to **AWD# K019303**.

American Airlines

American Airlines is providing 5-10% off of applicable fares, and 10%-15% on fares reserved before 60 days. Please identify for your discount with number **AN# 1558UJ** when calling **1-800-433-1790** to make reservations. In conjunction with American, Avis Car Rental will provide discounts with the reference number **AWD# B136000**.

Train

Amtrak provides train service to Salinas, CA, and bus service to Monterey (12 miles). Trains are available from Northern and Southern California. Please contact Amtrak for more information at **1-800-USA-RAIL (872-7245)** or **www.amtrak.com**. For groups of 20 or more, please call
1-800-872-1477.

Local Transportation

Local transportation to and from your airport destination and the conference location can be provided by:

Car Rentals in Monterey

Alamo (San Jose)	1-800-327-9633/www.goalamo.com
Avis	1-800-831-2847/www.avis.com
Budget	1-800-527-0700/ www.budgetrentacar.com
Enterprise	1-800-73682227/ www.pickenterprise.com
Hertz	1-800-654-3131/ www.hertz.com
National	1-800-227-7368/ www.nationalcar.com

Taxi

Yellow Cab	646-1234
Carmel Yellow Cab	626-3333

Limousine

A-1 Chartered Limousines Inc.	899-2707
Cypress West Sedan & Van Service	626-1234
Tom’s Livery Service	626-8119

Airport Shuttle Services

Monterey/Salinas Airbus 800-291-2877.
The Airbus provides transportation between San Francisco, San Jose and Monterey airports. Advance reservations recommended.

San Jose to Monterey - Fares: 1 person - $ 30.00; 2 people - 54.00; 3 people - 70.00. Shuttles pick up in SJC Terminal A across from the baggage claim to the right, departure side, at the County Transit Bus Stop. In Terminal C, shuttles pick up outside baggage claim to the left at the County Transit Bus Stop. Daily departures from San Jose Airport to Monterey and Salinas are scheduled for 10:30 AM, 1:30 PM, 4:30 PM, 7:00 PM, and 9:30 PM.

San Francisco to Monterey - Fares: 1 person - $ 35.00; 2 people - 58.00; 3 people - 70.00. At the Airport, pick up your shuttle on the lower level (baggage claim area) of any terminal, near the blue column on the center island. One way fare is $35.00, round trip $60.00. Discount for parties of 2 or more. 1-day return and group rates are available. Buses depart SFO daily for Monterey at 9:30 AM, 12:30 PM, 3:30 PM, 6:00 PM, and 8:30 PM. Approximate travel time to Monterey is 3 hours. The bus stops in Monterey at the Monterey Transit Plaza at the intersection of Pearl and Alvarado Streets in downtown Monterey by the Doubletree and Marriott Hotels.

Accommodations

Monterey Conference Center

The Monterey Conference Center offers an exceptional amount of meeting space for the ISCAS. The conference will utilize the Serra Exhibit Hall/Grand Ballroom, the Steinbeck Forum and the DeAnza Ballroom. The conference center is located adjacent the Doubletree and across the street from the Marriott Hotels.

Hotels

The 1998 ISCAS Conference has obtained very reasonable rates for both the Monterey Marriott and the Doubletree Hotel Monterey. Please review the registration form in the center of this advance program to obtain accommodations.

Addresses of the hotels are:

Monterey Marriott	**Doubletree Hotel Monterey**
350 Calle Principal	2 Portola Plaza
Monterey, CA 93940	Monterey, CA 93940
Phone: (408) 649-4234	Phone: (408) 649-4511
1-800-228-9290	1-800-222-8733 (TREE)
FAX: (408) 372-2968	FAX: (408) 649-3109
www.marriott.com/marriott/MRYCA	www.doubletreemonterey.com

Internet Access / Email

During the conference there will be locations available for computer and Internet access. These stations are reserved for attendees to contact their email, view conference related websites or view the ISCAS 98 CD-ROM to print selected publications.

Time Zone

During the end of May and early June, the Monterey Peninsula follows the Standard Pacific Time Zone, or 8 hours following Greenwich meantime. We are 3 hours behind the U.S. East Coast and 18 hours behind Japan and 10 hours behind Western Europe.

Climate

The climate during May and June is very pleasant, with highs in the mid 60's F (16 C) and lows in the upper 40's F (4 C). May and June are in the early part of the dry season for central California. Rain is a rarity, but fog can be expected in the mornings. A jacket is recommended in the evenings, especially close to the bay.

Language

The primary language is English; however for the international visitor, many international languages are spoken in the city. Monterey is home for the Monterey Institute of International Studies and the U.S. Defense Language Institute. For interpreter information contact:

Monterey Institute of International Studies	(408) 647-4130
Monterey Language Academy	(408) 649-8122
Defense Language Institute	(408) 242-5844

Emergencies/ Medical

For all emergencies, call 911 for Fire, Police or Ambulance.

Hospital

For emergencies, the Community Hospital of the Monterey Peninsula is located just off of Route 1 south at the Pebble Beach exit.

Community Hospital of the Monterey Peninsula (CHOMP)
23625 W.R. Holman Hwy
General Information 408-624-5311

Currency

Currency exchange is located can be provided at: Marriott Front Desk (for guests) and Doubletree Front Desk (for guests)

Local Attractions

The Monterey Peninsula has too many attractions for us to mention in this program. To obtain more than is provided here, please view the website **http:\\www.monterey.com** for a wealth of local information.

Monterey

Visit the downtown historic sites, Colton Hall famous for the signing of the California Constitution, Robert Louis Stevenson's house, the Custom's House, and the Maritime Museum to name a few. Enjoy dining downtown at Fisherman's Wharf, or just about anywhere.
On Tuesday's from 4PM to 7PM downtown Monterey closes Alvarado St. for buyers and spectators to stroll among more than 100 booths. This event features artisans, prepared food vendors, ethnic clothing, musicians, bookmobile, face-painting, old books, and of course, fruits and vegetables, flowers, baker's alley, meat, nuts, honey and eggs. For you bargain hunters, the Monterey Flea Market is open all day Tuesday and Wednesday at the Monterey Fairgrounds, located just south of Fremont towards the Airport.

Carmel-by-the-Sea

On the other side of the hill from Monterey, Carmel, with a population of 5,000 residents, plays host to thousands of visitors each year. By the 1920's, Carmel had already achieved its international reputation as an "artists' colony." Now its biggest attractions are the downtown shopping district and its beautiful beaches. You won't find many sidewalks, streetlights, neon signs or mailing addresses, but you will find specialty shops, boutiques, art and photography galleries and great restaurants. Visit the quaint shops in the Carmel Barnyard or stop in the Hog's Head Inn and "Make my (your) day".

Pacific Grove

Better known by locals as "America's last hometown," Pacific Grove is also known for its thriving population of Monarch butterflies, but by June, they will have left for the summer. A walk through the residential neighborhoods reveals many well-preserved, turn of the century, Victorian homes. History buffs can visit the Point Piños Lighthouse, the oldest operating facility of its kind on the California coast. The Monterey Bay recreational trail passes by Lover's Point, offering many opportunities to view sea otters, sea lions and occasionally passing whales.

Pebble Beach

A gated community located between Carmel-by-the-Sea and Pacific Grove. Its 17-Mile Drive draws hundreds of visitors daily where views of the ocean, cypress trees, fabulous houses and deer, not to mention the world's most dramatic golf courses, are breathtaking. Visit the shops and dining at the Pebble Beach Lodge or the Inn at Spanish Bay

Big Sur

Visit just 25 miles south of Monterey where the mountains meet the ocean. Examine the Redwood forests or dine overlooking the Pacific.

Moss Landing

This seaside port about 20 miles north of Monterey hosts a great find for the antique hunter or a good reason to go salmon fishing on the bay.

Point Lobos State Park

Located 3 miles south of Carmel on Highway 1 provides breathtaking views. Deriving its name from the offshore rocks at Punta de los Lobos Marinos, Point of the Sea Wolves, where the sound of the sea lions carries inland, the reserve has often been called "the crown jewel of the State Park System." For those lovers of the outdoors, you shouldn't miss this jewel. (http://pt-lobos.parks.state.ca.us)

Useful Information

Conference Venue:
Monterey Conference Center
1 Portola Plaza
Monterey, CA 93940
Phone: (408) 646-3770

Useful email addresses:

Technical Program	tchair@iscas.nps.navy.mil
Special Sessions	special @iscas.nps.navy.mil
Registration	register@iscas.nps.navy.mil
Secretariat	webmaster@iscas.nps.navy.mil

Hotels:

1. Monterey Marriott		(408) 649-4234
		(800) 228-9290
	FAX:	(408) 372-2968
2. Doubletree Hotel Monterey		(408) 649-4511
		(800)222-8733
		(TREE)
	FAX:	(408) 649-3109

Conference Secretariat:
Code EC
833 Dyer Road, Room 437
Naval Postgraduate School
Monterey, CA 93943-5121
Phone: (408) 656-5073
FAX: (408) 656-5074
Email: webmaster@iscas.nps.navy.mil
http://www.iscas.nps.navy.mil

ISCAS '98 Registration

Symposium Registration will be held in the Portola Lobby of the Monterey Conference Center. All symposium attendees must register and carry their name tag at all times. The registration desk at the conference will be open beginning Saturday, 30 May 1998 from 6:00 PM – 9:00 PM. It will be open on Sunday, 31 May, 1998, from 7:30AM – 5:00 PM and on each of the following three days.

ISCAS '98 Computer Room

The **Portola Room** by the Double Tree registration desk, is equipped with several PC stations. These stations are available to the Symposium participants. Electronic copies of the ISCAS'98 Proceedings.are available for viewing and printing. All PC's are networked for web browsing and electronic mail.

ISCAS ’98 Proceedings and CD-Rom

All conference registration will include one copy of the complete ISCAS ’98 Proceedings on CD-Rom. Hard coy Proceedings are published in the six volumes listed below. The complete Proceeding is available for $180 at the conference or a single volume for $40 per volume. An extra CD-Rom is also available for $60. Stop by the ISCAS ’98 Proceedings desk of the Portola Lobby.

VOL I – Analog Circuits & Systems
VOL II – VLSI
VOL III – Neural Networks – Circuit Theory & Power Systems
VOL IV – Multimedia Systems – Communication Circuits & Systems
VOL V – Digital Signal Processing I & II
VOL VI – Computer Aided Design – Communication Networks - Applications

“FREE” IEEE Membership

Non-members can become Members of IEEE at absolutely no cost
[Stop by the IEEE Membership desk in **DeAnza Room**]

Those who are not member of IEEE and register for ISCAS ‘98 at non-member rates are being offered a rare and one-time opportunity to become regular members of IEEE for one year and the membership is FREE. They will also get a free one-year membership in the Circuits and Systems Society and subscription to one of its *Transactions* chosen by the non-member. All that a non-member has to do is fill a special application form that will be distributed during the registration at ISCAS ’98 and mail it to IEEE along with the registration receipt. The Circuits and Systems Society is one of the only two societies which has been granted permission by IEEE to recruit new members at no cost to them. All non-members att3ending ISCAS ’98 are urged to make use of this rare opportunity to become IEEE members absolutely free and enjoy the full benefits of regular membership for one year. For more details, contact Dr. B. A. Shenoi at <bshenoi@cs.wright.edu>.

Author’s Breakfast

All author’s are invited to the Author’s Breakfast on the day of their paper presentation, to meet with the session chairperson and the other session authors. Breakfast will be continental style and will run from 7:00am until 8:00am on Monday through Wednesday in the Ferrante’s Restaurant at the top of the Marriott. Paper presentation will be limited to 20 minutes in addition to 2 minutes for questions. If you have not filled out the short biographical data form, please do so and hand it in to your session chair at this breakfast.

Coffee and Refreshment Breaks

Coffee breaks are scheduled every morning from 10:30am to 11:00am and refreshments breaks are scheduled in the afternoon from 3:30pm to 4:00pm. Breaks will be located in the exhibit area at the DeAnza Ballroom. Pastries and fruits will also be available during the morning and afternoon breaks.

Exhibits

Several publishers will exhibit and display their books and products in the exhibit area in the DeAnza Ballroom throughout the conference.

Author’s Preparation Room

The **Cottonwood II** room has been set aside for Authors to prepare their presentations. Audiovisual equipments are available in the room. Instructions for Presentation are on the following two pages.

Guidelines for Authors of Lecture Presentations

Lecture sessions provide an opportunity for presentation of your work to a large audience in a short time. Because lecture sessions are synchronous in nature and some attendees plan to move among sessions to catch the papers of their interest, we urge you to adhere to the time allocated to you. Since the time available to present your work is rather short, you need to prepare your presentation materials with utmost clarity and effectiveness. Please follow the following guidelines to help make the lecture sessions successful.

Lecture Preparation

1. All lecture session rooms will be equipped with an overhead projector (for viewgraphs or transparencies) and a 35 mm projector (for slides).
2. Please prepare your viewgraphs/slides in advance. No materials or equipment will be available at the symposium for preparing your presentation materials at the last minute. We request you not to use hand written presentation materials.
3. Some of the lecture sessions are held in large lecture halls. Size of lettering and clarity of presentation materials are important. For letter size, we recommend times new roman with font size 24 points or larger.
4. Please keep in mind that your typical audience can only absorb about six major points during your short presentation. As you prepare your materials, your job is to select those six key points and present them clearly and effectively.
5. To cover those six points, you should be using no more than eight viewgraphs/slides. Make them simple and clear. By cramming too many lines on a viewgraph, you will only lose your audience.
6. Use graphics, schematic diagrams, and figures to make the presentation effective. Keep the text to the minimum possible.
7. Your lecture will typically have the following sections: A brief overview of the work reported in the paper; Significant results; Impact of your results on relevant applications; Conclusion.
8. Please rehearse your presentation prior to coming to the symposium. You will only have 15-17 minutes to present you work, and you will be able to speak between 1000 and 1500 words during this period.

Lecture Presentation

1. Please plan to arrive at the assigned lecture room ten to fifteen minutes prior to the start of the session (not just your lecture) to introduce yourself to the session chair and to make sure that the needed presentation equipment is available in the room.
2. All regular full-lecture sessions have 8 papers (half-lecture sessions have 4 papers). Lecture presentation slots are 22 minutes long. Please limit your presentation to 15-17 minutes while leaving the remaining time for questions and comments from the audience.
3. A few special full-lecture sessions have 9 papers (half-lecture sessions have 5 papers). The lecture presentation slots in these sessions are 19 minutes long. Please limit your presentation to 12-14 minutes while leaving the remaining time for questions and comments. These sessions might run a few minutes longer than the other sessions. Your session chair will provide specific instructions on the exact timing of papers at the start of the session.
4. Please do not read directly from the viewgraphs or slides. Use them only as a guide. We DO NOT recommend reading from a prepared speech. Nevertheless, you (especially, our foreign speakers) might wish to prepare written opening and closing sentences.
5. Non-author (substitute) presentations are not highly encouraged but acceptable if the real authors cannot be present at the symposium. The substitute presenters must be sufficiently familiar with the material being presented in order to be able to answer questions from the audience. Also, the substitute presenter must contact the session chair ahead of the scheduled session time to apprise him/her of the change.

Instructions for Authors of Poster Presentations

Poster sessions provide an opportunity for interactive and in-depth technical presentation. Because poster sessions are asynchronous in nature, attendees can sample the papers of their interest at their convenience and without concern for presentation schedule conflicts. Please follow the following guidelines to help make the poster sessions successful.

Poster Preparation

1. Poster boards of size 8 feet wide by 4 feet high (240 cm x 120 cm) will be available in the assigned rooms. Push tacks will be provided to bind the poster to the board.
2. Please prepare your poster in advance. No materials will be available at the symposium for preparing your poster at the last minute.
3. Include only key points of your paper in the poster. Please do not post the enlarged copies of your camera-ready paper on the board; it is a well understood fact that such posters are not well received by the symposium attendees.
4. Design your poster to attract attention. Large lettering, graphics and color will help. For letter size, we recommend times new roman with font size 32 or larger. Minimize the use of text. Use diagrams and figures instead of text as appropriate. No handwritten posters please.
5. If you are using multiple sheets to make up your poster presentation, please plan on arranging the flow in a columnar (downward) fashion. Start at the top left and end at the bottom right.
6. Make your poster as self-explanatory as possible. This will give the interested attendees a chance to browse through your presentation prior to asking detailed questions, if any.
7. Your poster will typically have the following sections: A brief overview of the work reported in the paper; Significant results; Impact of your results on relevant applications; Conclusion.
8. Please rehearse your presentation prior to coming to the symposium.

Poster Presentation

6. Please set up your poster at least five minutes prior to the start of the session.
7. Authors of all ODD numbered papers in a poster session are required to be physically present by their posters BEFORE the coffee break; accordingly, authors of all EVEN numbered papers are required to be present by their posters AFTER the coffee break.
8. Prepare one (overhead projector) transparency for a one minute overview of your presentation at the start of the session. The session chair will introduce you to the audience, so please do not repeat your name and affiliation; just give a quick overview without any formalities. Authors of ODD numbered papers will present their one-minute overviews at the start of the session (before the coffee break) while authors of EVEN numbered papers will do the same (at the start of the session) after the coffee break.
9. As attendees visit your poster, please be prepared to give a short (several minutes) presentation of your work. You will need to repeat this several times as attendees pass through.
10. We encourage more than one author to be present at the poster (for papers with multiple authors). Experience shows that more successful poster presentations have at least two authors present to share the load of presenting and interacting with the audience.
11. Authors are encouraged to bring additional audio/visual aids (hand-held, battery-operated) to enhance the presentation.

ISCAS ’98 Side Meetings

Date	Day	Start	End	Meeting	Mtg Chair	Room Location
29-May-98	Friday	3:00 PM	7:00 PM	BOG Tech Act.	Bayoumi	Dana
30-May-98	Saturday	8:00 AM	3:00 PM	ExCom	DeFigueiredo	Colton II
30-May-98	Saturday	3:00 PM	7:00 PM	PAC	Shenoi	Ferrante I
30-May-98	Saturday	4:00 PM	7:00 PM	BOG Div Conf	Sheu	Ferrante II
30-May-98	Saturday	4:00 PM	7:00 PM	BOG Div Pub	Huang	Ferrante III
30-May-98	Saturday	4:00 PM	7:00 PM	TC Chairs Mtg	Bayoumi	Colton I
31-May-98	Sunday	9:00 AM	6:30 PM	BOG	DeFigueiredo	San Carlos IV
1-Jun-98	Monday	12:30 PM	2:00 PM	ISC APCCAS	Takagi	San Diego
1-Jun-98	Monday	12:30 PM	2:00 PM	VLSI Sys + Appl Tech.	Sheu	Los Angeles
1-Jun-98	Monday	12:30 PM	2:00 PM	Analog	Fiez	Santa Monica
1-Jun-98	Monday	12:30 PM	2:00 PM	Visual	Li	Redwood II
1-Jun-98	Monday	12:30 PM	2:00 PM	Non-linear	Trajkovic	Redwood I
1-Jun-98	Monday	5:30 PM	7:00 PM	Multimedia	Sheu	Redwood I,II
2-Jun-98	Tuesday	12:30 PM	2:00 PM	ISCAS 2000	Hasler	Los Angeles
2-Jun-98	Tuesday	12:30 PM	2:00 PM	DSP	Nguyen	Santa Monica
2-Jun-98	Tuesday	12:30 PM	2:00 PM	TCAS-I & -II Ad-Hoc Comm	Huang	San Francisco
2-Jun-98	Tuesday	12:30 PM	2:00 PM	Neural	Salam	Redwood I
2-Jun-98	Tuesday	12:30 PM	2:00 PM	Editorial TCSVT	Zhang	Redwood II
2-Jun-98	Tuesday	12:30 PM	3:00 PM	ISCAS 99	Mikhael	Cottonwood I
2-Jun-98	Tuesday	12:30 PM	2:00 PM	Power Systems	Chung	San Diego
3-Jun-98	Wednesday	12:30 PM	2:00 PM	Editorial TCASII	Sanchez-Sinencio	Cottonwood I
3-Jun-98	Wednesday	12:30 PM	2:00 PM	Editorial VLSI	Sheu	San Diego
3-Jun-98	Wednesday	12:30 PM	1:00 PM	Reg. 8/10 Chairs	Davies/Hellestrand	Redwood I
3-Jun-98	Wednesday	1:00 PM	2:00 PM	Reg. 10 Chairs	Hellestrand	Redwood II
3-Jun-98	Wednesday	1:00 PM	2:00 PM	Reg. 8	Davies	Redwood I
3-Jun-98	Wednesday	2:00 PM	3:00 PM	TCAS-II '98 Spec	Maloberti	Cottonwood I
4-Jun-98	Thursday	8:00 AM	2:00 PM	ISCAS Steering Com	Sheu/Michael	Los Angeles

The 1999 IEEE International Symposium on Circuits and Systems, ISCAS ’99

The 1999 IEEE International Symposium on Circuits and Systems will be held at the Renaissance Orlando Resort in Orlando. Florida, on May 30 – June 2, 1999. The **CALL FOR PAPERS** can be found on the next page.

PRESYMPOSIUM TUTORIALS

Presymposium Tutorial registration and reception are scheduled for 6:00PM – 9:00PM on Saturday, May 30, 1998, in the Portola Lobby.

Full Day Tutorials - Sunday May 31, 1998 (8 AM – 5 PM)

1. Introduction to Electronic Image Processing

Presenter: Arthur Weeks

University of Central Florida

1.. Many disciplines of science and engineering acquire and analyze images on a routine basis. Typically these images must be processed so that important features can be measured or identified. It is the goal of this short course to introduce the fundamentals of electronic image processing to scientists and engineers that must know how to manipulate images that have been acquired and stored within a digital computer. This course will cover the following topics:

a. Image storage, acquisition, and digitization
b. Image transforms such as Fourier, Hough, Walsh, Hadamar, and Discrete Cosine
c. The difference between the various types of linear and non-linear filters and when to use each
d. The difference between several types of noise in the degradation of an image
e. Image segmentation techniques and how these techniques are used to extract objects from an image

Text: *Fundamentals of Electronic Image Processing*, A. Weeks, SPIE and IEEE Press, 1996.

2. Integrated CMOS Image Sensors: Theory and VLSI Implementation

Presenter: Cyrus Afghahi

INTEL Corporation

Presenter: Mohammed Ismail

Ohio State University

Co-sponsored by the CAS Analog Signal Processing Committee and the CAS Technical Committee on Multimedia Systems and Applications

The advent of submicron CMOS technology and advances in CMOS mixed analog/digital techniques have enabled the development of integrated CMOS image sensors. Innovative applications of such sensors include modern multimedia systems, computer peripherals, portable consumer products, telemedicine etc. The advantages of CMOS image sensors are low voltage, low power (LV/LP) operation, compatibility with standard cheap digital CMOS processes and the possibility of random access and integration of various functions and algorithms on the same chip. This intensive course will introduce the basics in the theory and design of integrated CMOS image sensors. The coverage will be given at an introductory level. Students and newcomers are particularly encouraged to participate.

This course will enable you to understand specification and device physics related to CMOS processing. Also understand system specification for SNR, frame rate, linearity, A/D concepts for integrated CMOS imagers, theory and design of correlated double sampling, basic VLSI LV/LP circuit techniques for imager design and issues in testing integrated CMOS imagers.

4. What You Want to Know about Multimedia Circuits and Systems

Presenters: Ming-Ting Sun
University of Washington
Bing Sheu
University of Southern California
Chung-Yu Wu
National Taiwan University
Tsuhan Chen
Carnegie Mellon University

A. Network Technologies for Multimedia Applications

Video on demand, distance learning, video-conferencing, and digital library, are just some examples of multimedia applications which will have a large impact to our society. However, before we can realize the full potential of these multimedia services, we have to address the challenge of how to deliver multimedia applications over networks cost-effectively, ubiquitously, and with sufficient quality. Several access network technologies such as POTS, ISDN, ADSL, HFC, FTTC, MMDS, and LMDS have been proposed for delivering multimedia services to the mass market. There are also significant activities in ITU-T, IETF, and ATM Forum to propose standards for multimedia applications over ATM networks and the Internet. In this tutorial talk, we will review the terminologies, features, advantages, limitations, various issues such as Quality of Service, and progresses for these networking technologies. We will provide the audience with an overall picture of multimedia networking technologies and research issues/opportunities in the active area of multimedia networking.

B. Multimedia Circuits and Systems for Practical Applications

Interaction and merging among the computer, communication, and entertainment industries gave birth to the multimedia era. Multimedia has the potential of becoming one of the most powerful forms of searching for information, communicating ideas, and experiencing new concepts of any form of communication or networking. Many business opportunities are connected through the incredible "Information Superhighway - the Internet." As deep-submicron microelectronic technologies continue to advance, the executable system algorithms and software tools become more sophisticated. Moreover the hardware becomes cheaper to construct, and the potential for multimedia systems and machines to be commonly used is tremendous. Therefore, the computer, telecommunication, entertainment, cable, and other consumer electronics industries are racing to this emerging market. Knowledge and results achieved by researchers/engineers in the Circuits and Systems Society of IEEE have been making a significant impact on the development of multimedia products and machines. This talk will describe the trends of development in design technologies and emerging products in multimedia. The underlying algorithms, architectures, and circuit techniques will be presented. Selected simulation and measured results will be used to illustrate how the research and development are accomplished.

C. Advanced CMOS Imaging Technology for Multimedia Video

Advances in submicron VLSI technologies have made possible the integration of sensing devices and readout circuitry on the same microchip for very inexpensive camera-on-chip solutions. Such a break-through CMOS camera chip is indispensable in future multimedia-based personal computers and portable electronic products. With the high integration level, separate frame-grabber hardware is no longer needed because the CMOS implementation allows random access, and holding of the image data on the chip directly. In this talk, we will describe the architecture of the CMOS imager, the sensing device, and various read-out circuit topologies. Practical consideration of the noise reduction techniques associated with the read-out circuits will be emphasized. The intelligent vision techniques to enhance on-chip imaging capability will also be presented. Finally, the applications to multimedia video will be discussed.

D. New Developments in Standards for Video Coding and Multimedia Communications

We will provide an in-depth yet tutorial-valued review of recent progress in video coding and multimedia communications. In the video coding aspect, state-of-the-art coding standards will be presented. Emphasis will be given to a number of emerging standards, including H.263 Version 2 and MPEG-4. In the communication aspect, special considerations for sending multimedia over IP, wireless, and ATM networks, such as error resilience, will be discussed.

5. Coding and Compression of Text, Waveforms and Images

Presenter: Samuel Stearns
Sandia National Laboratories
Presenter: Neeraj Magotra
University of New Mexico

This is a full-day tutorial on text, waveform and image compression. It is designed to teach:
(a) Up-to-date coding and compression procedures,
(b) the application of these procedures to different types of data and signals, and
(c) enough basic theory to enable the student to modify and improve standard procedures in specific applications, and to develop new techniques.

COURSE OUTLINE:

The course will cover the following topics, more or less in the order given, over a course period of 6-8 hours:
Basic coding and compression principles:
(1) Reducing avg. number of bits/symbol; maximizing entropy.
(2) Producing statistically independent symbols; decorrelation.
- Definitions of compression applications to be covered:
- Data types (text, waveforms, images, video) and techniques (lossless compression, lossy compression).
- Summary of coding and compression techniques to be covered:
- Run-length coding, Predictive coding, Transform coding, Huffman coding, and Lempel-Ziv-Welsh coding .
- Codebook techniques: Arithmetic coding
- Lossless coding and compression of data files in general including:
- Run-length coding, Huffman coding, Arithmetic coding, Fixed and adaptive implementations, LZW and arithmetic coding, Lossless predictive coding and Lossless transform coding.

Also Compressibility, Compression of waveform data (music, speech, telemetry, etc.) and digital image and video data will be discussed. Compression software will be provided with this course.

6. Recent Progress in Modeling and Simulation of High Speed VLSI Interconnects

Presenter: Michel Nakhla
Carleton University

The intense drive for signal integrity has bee n at the forefront of rapid and new development in CAD algorithms. With increasing demands for high signal speeds coupled with a decrease in feature size, interconnect effects such as signal delay, distortion and crosstalk become the dominant factors limiting overall performance of VLSI systems. On the other hand, interconnect structures can be diverse and present at any of the hierarchical packaging levels including integrated circuits, printed circuit boards, multi-chip modules and backplanes. If not considered during the design stage, interconnect effects can cause logic glitches, which render a fabricated digital circuit inoperable, or they may be able to distort an analog signal such that it fails to meet specifications. Since extra iterations in the design cycle are costly, accurate prediction of these effects is a necessity in high-speed designs. Although conventional CAD tools such as SPICE are used routinely by many engineers for analog simulation and general circuit analysis, these tools do not handle adequately the new emerging challenges of interconnect effects. This lead to intense research during recent years to develop efficient techniques for accurate signal integrity analysis associated with high-speed interconnects.

Recently proposed model-reduction techniques such as Asymptotic Waveform Evaluation (AWE), Complex -Frequency Hopping (CFH) and Krylov space-based methods have proven useful in the analysis of large interconnect structures containing lossless and lossy high-speed interconnects with linear or nonlinear terminations. At a CPU cost of a little more than one DC analysis, these techniques are 2-3 orders of magnitude faster than conventional methods.

This tutorial presents an overview of interconnect modeling/simulation strategies with emphasis on diverse algorithms and applications of model- reduction techniques. The underlying basic concepts will be demonstrated by several practical examples.

The tutorial is intended for developers of CAD tools and for circuit designers as well. It is presented in an easy to understand style and prior background in this area is not required. The first part of the course covers the basic principles of circuit simulation. The second part focuses on issues and analysis techniques related to high-speed circuits and interconnects. Various interconnect models will be considered including RC/RLC lumped, distributed, full-wave, measured

and EMI-based. The basic principles of model-reduction techniques will be described in details together with their extension to some frequently-encountered practical situations such as simulation of subcircuits characterized by measured S-parameters and frequency-dependent components (e.g. resulting from skin and proximity effects). Applications cover wide spectrum of implementation hierarchy including chip, multichip modules, packages and printed circuit boards.

Half Day Tutorials - Sunday May 31, 1998

12. VLSI Architectures for Video and Data Communications

Presenter: Keshab Parhi

University of Minnesota

This tutorial addresses approaches to implementation of next generation signal and video processors necessary for multimedia communication systems. High level transformations will be reviewed. Low power design aspects will be particularly emphasized. Computer arithmetic implementation styles will be considered. Both video and data communication systems will be addressed. Implementation approaches for both dedicated and programmable styles will be considered. Examples such as cable modems and video styles will be considered. Examples such as cable modems and video compression will be addressed. Topics include:

A. Architectural Transformations - high level transformations such as pipelining, retiming, parallel processing, algorithmic and numerical strength reduction, folding and unfolding and their impact on area-speed-power tradeoffs. Power reduction by reduction of supply voltage, capacitance and switching activities.

B. Arithmetic Architectures - high speed and low-power multiplication and addition in two's complement, and redundant number systems, carry-save and canonic signed digit numbers. Implementation styles such as bit- and digit-serial methodologies.

C. Video Compression Systems - architectures for DCT, motion estimation and VLDs, implementation using dedicated and media and MMX programmable DSPs.

D. Data Communication Systems - Architectures for Viterbi decoders, finite field and error control coders, cable modems. Trends in programmable DSPs for wireless systems.

Technical Program Committee

Co-Chairs

Murali Tummala
Naval Postgraduate School
tchair@iscas.nps.navy.mil

Kenneth Laker
University of Pennsylvania
laker@iscas.nps.navy.mil

Track 1: Analog Circuits and Signal Processing
Randall L. Geiger
Iowa State University (Chair)
rlgeiger@iastate.edu

Track 2: Circuits and Power Systems
Wai-Kai Chen
University of Illinois at Chicago (Chair)
wkchen@eecs.uic.edu

Track 3: Computer aided Design
Ibrahim Hajj
University of California, Berkeley
(on leave from University of Illinois at Urbana) (Chair)
hajj@ic.eecs.berkeley.edu

Track 4: VLSI
Gordon Roberts
McGill University, Canada (Chair)
roberts@macs.ee.mcgill.ca

Track 5: Neural Systems
Jan Van der Spiegel
University of Pennsylvania (Chair)
an@ee.upenn.edu

Track 6: Digital Signal Processing I
P.P. Vaidyanathan
California Institute of Technology (Chair)
ppvnath@systems.caltech.edu

Track 7: Digital Signal Processing II
M.N.S. Swamy
Concordia University, Canada (Chair)
swamy@ece.concordia.ca

Track 8: Multimedia and Video Technology
Bing Sheu
University of Southern California (Chair)
sheu@pacific.usc.edu

Track 9: Communication Circuits and Systems
Donald F. Gingras
SPAWAR Systems Center, San Diego (Chair)
gingras@spawar.navy.mil

Track 10: Computer Communications
Chung-Sheng Li
IBM T. J. Watson Research Center (Chair)
csli@watson.ibm.com

Track 11: Applications
Xiaoping Yun
Naval Postgraduate School
yun@ece.nps.navy.mil

Technical Program Committee Members

M.O. Ahmad (member, Track 7)
Concordia University, Canada
A. Antoniou (member, Track 7)
University of Victoria Canada
Lex. A Akers (member, Track 5)
University of Texas at San Antonio
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Imperial College UK,
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Northwestern
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Ecole Polytechnique, Canada
Rolf Schaumann (member, Track 2)
Portland State University
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Carleton University, Canada
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University of Washington, Seattle
Ken Suyama (member, Track 4)
Columbia University
K. Thulasiraman (member, Track 2)
University of Oklahoma
Chung-Yu Wu (member, Track 8)
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Sun, Ming-Ting
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Thanachayanont, Apinunt
Thanos, Stouraitis
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Thulasiraman, K.
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Toumazou, C.
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Tsai, Ching-Han
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Tse, Michael C. K.
Tzou, Kou-Hu
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van Staveren, Arie
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Zefran, Milos
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Zeng, Fan-Gang
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Zhou, Joe P
Zhu, Weiping
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ISCAS ’98

1998 IEEE
International Symposium on Circuits and Systems

Technical Program and Abstracts

Session Rooms	Sunday	Session Numbers	Monday, June 1		Tuesday, June 2				We
			Plenary Speaker- 8:05-8:45 **Mr. Jack Harding** **Cadence Design Systems**		Plenary Speaker – 8:05 – 8:45 **Dr. Robert Trew** **ODDRE**				**Plena** Dr. Greg Pap **Su**
			MA	**MP**	**TA/TB**	**TP**			**WA/WE**
			9:00 – 12:30	**2:00 – 5:30**	**9:00 – 12:30**	**2:00 – 3:30**	**4 –5:30**		**9:00 – 12:3**
Colton I	**SC 1**	**1**	Parameter Estimation	Multidimensional Signal Processing	Filter Banks & Wavelets	Adaptive SP II	**Panel Session I - Government Funded Research – Serra Ballroom II**	**Panel Session II – Teaching Circuits & Systems in the 21st Century – Steinbeck Forum**	Adaptive Signal Proc
Colton II	**SC 2**	**2**	Single-rate & Multirate Filters	**Opti of Subband Coders based on the Input**	**Model., Anal. & Design Switching Converters**	**Coding of Arbit.-Shaped Objs**			**Steerable Filte Application**
Colton III	**SC 5**	**3**	**NN for Intelligent Signal Processing**	**Memory, Adaptation & Learning**	NNI: Algorithms & Computation	NNII: Implement Issues			Nets Biological Com Fuzzy Logic
Ferrante I	**SC 4**	**4**	Image Processing & Coding	Multimedia Systems & Process	Speech &Video Processing	Image & Video Proces			Image & Video Proc
Ferrante II	**SC 6**	**5**	Signal Processing Comms I	Equal/Mod/ Decoding	**Communicating with Chaos I**	SP for Comms II			Wireless/Mob Communicatio
Ferrante III	**SC 12** **SC 13**	**6**	Low-Power IC Techniques	Circuit Techniques Wireless Apps	Logic Device	C&S for Comm Nets I			Dig Circuit Issues / D
Bonzai I		**7**	Chaos & Application	Linear Circuits	Nonlinear Ntwk & Systems	Analog VLSI			Power Electronics
Bonzai II		**8**	Data Converters	Continuous-Time Filters	Amplifiers I				Amplifiers I
Bonzai III		**9**	Sym. Anal. Meths &Appl. to Anal. Circuit Design	Hi-Speed Communications Circuits	Logdomain Filters	**Comm with Chaos II**			Switched-Capacitor T
San Carlos I		**10**	Low Power Digital Circuit Design	Interconnect Modeling & Design	Oversampled Data Converters	Circuit Simulation			**Communicating wi III**
San Carlos II		**11**	VLSI Circuits for MM Signal Processing	**Multi-Sensor Data Fusion**	**DSP for Hearing Aids**	Robotics			VLSI Layout & T
San Carlos III		**12**	VLSI Digital Circuits	Power Distribution Systems	Analog Circuits Design	Feedback Systems			**Sys & Appls Next G Internet**
Serra Ballroom – Back I		**13**	**Communications Circuits**	**Image & Video Processing I**	**Adapt. SP I** / **DSP Implt**	**MM Processing**			**Digital Filter D Implementati**
Serra Ballroom – Back II		**14**	**Circuits & Power Systems I**	**VLSI I**	**VLSI II** / **Circuit& PS**	**Oversampl & S-D I**			**VLSI Arch, Algori CAD**
Serra Ballroom – Back III		**15**	**Analog Filters**	**Analog & Signal VLSI Design**	**CAD I**	**Sensors & Circuits**			**CAD II**

SC – Short Course **Special** **Poster**

MONDAY MORNING -- JUNE 1, 1998

Plenary Monday

8:05am – 8:45am (Serra Grand Ballroom)

Mr. Jack Harding – President and CEO, Cadence Design Systems, Inc.

Title: System-On-A-Chip and the Path to Design Realization

MAA1 – Parameter Estimation

Chair: Eugene I. Plotkin

Concordia University

9:00 am – 12:30pm - ***Room: Colton I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA1-1 -- On the Harmonic Analysis of Speech

Stylianou, Ioannis G., *AT&T Labs*

This paper focuses on the analysis of the periodic part of speech signals using harmonic models. Three different models are discussed with respect to their effectiveness in modeling the periodic (harmonic) part of speech. The non-periodic part of speech is then obtained by subtracting in the time domain the harmonic part the original speech signal.

MAA1-2 -- Parameter-Free Structural Modeling: A Contribution to the Solution of the Separation of Highly Correlated AR-Signals

Plotkin, Eugene I. and Swamy, M.N.S., *Concordia University*

This paper develops the concepts and properties of composite parameter structural (CPS) modeling, and shows how such properties can be exploited for the separation of very highly correlated autoregressive signals. A CPS model recently developed and used to represent a signal of a given structure (given order of an AR model) but of unknown, or partially unknown, parameters, is investigated. The main feature of the described CPS model is the utilization in its design of almost ideal null filters, resulting in low noise sensitivity. The performance of the proposed algorithms is analyzed using computer simulations.

MAA1-3 -- A New Approach For Coherent Direction-Of-Arrival Estimation

Lai, W.K. and Ching, Pak-Chung, *The Chinese University of Hong Kong,*

Eigen-decomposition based methods for direction-of-arrival (DOA) estimation are known to perform poorly when the signals are coherent or highly correlated. Pre-processing techniques such as spatial smoothing and coherent source detection are commonly used to tackle the problem. But these methods often require non-trivial formation of subarrays or a high computation complexity. In this paper, we present a novel method that is capable to resolve the DOAs for coherent signals without using either source detection or spatial smoothing. Furthermore, additional number of sensors is not needed.

MAA1-4 -- Non-Minimum Phase FIR System Identification Using Cumulants with Selected Orders

Li, Wei and Siu, W.C., *The Hong Kong Polytechnic University*

In this paper, we address the problem of identifying the parameters of a nonminimum phase FIR system from the cumulants of some noisy output samples. The system is driven by an unobservable, zero-mean, independent and identically distributed (i.i.d) non-Gaussian signal. The measurement noise may be coloured MA or ARMA Gaussian process. For this problem, there have been a number of linear cumulant-based approaches. But these algorithms fail to perform the estimation due to using the correlation of outputs. In this paper, we propose two methods, one is to employ two arbitrary adjacent order cumulants, while the other is to use two arbitrary order cumulants together with the cumulant with the order equal to the sum of the orders of the two arbitrary cumulants. Simulation experiments, by comparing our algorithms with other five existing algorithms, prove that the first algorithm indeed produces the best estimates in terms of the mean, the standard deviation and the root mean-square error of the parameter estimates when the signal-to-noise ratio is very small.

MAA1-5 -- A Subspace Method For Blind Single Channel Identification Using Redundancy-Transform in Transmitters

Choi, Jinho, *LGIC*

We consider a subspace method to blindly estimate finite impulse response channels using redundancy-transform in transmitters. It is shown that the subspace method has a quadratic cost function. From this, we may have computationally efficient methods to estimate of the channel vector. We also consider sufficient conditions of channel identifiability.

MAA1-6 -- On Implementation of a Least-Squares Based Algorithm for Noisy Autoregressive Signals

Zheng, Wei Xing, *University of Western Sydney*

A least-squares (LS) based algorithm for noisy autoregressive signals is recently proposed, which needs neither to prefilter noisy data nor to

perform parameter extraction. In this paper, a more computationally efficient procedure for estimating the measurement noise variance is developed, and then an efficient implementation of the algorithm is presented. It is shown that this better way of implementation can considerably reduce the computational requirement of the LS based algorithm.

MAA1-7 -- Parallel Computation of SVD for High Resolution DOA Estimation

Feng, Gang and Liu, Zemin, *Beijing University of Posts &Telecom*

In the study of array signal processing, the extensively researched MUSIC (Multiple Signal Characterization) algorithm can be realized based on SVD(Singular Value Decomposition) and many advantages are expected to be achieved. In the application of SVD, how to compute SVD on a parallel array becomes a key issue. In this paper, we discussed several SVD algorithms and their implementation on array processing. Detailed analyses demonstrate some modifications of Hestenes SVD method and Franklin SVD algorithm can make them more suitable for array processing since the array architecture may be substantially simplified.

MAA1-8 -- Performance Analysis of a Class of Cyclic Weighted Subspace Fitting Method of Direction Estimation for Cyclostationary Signals

Yu, Hongyi and Zheng, Bao, Xidian University

Based on the asymptotic statistic characteristics of cyclic correlation matrices, an analysis of the performance of a class of cyclic weighted subspace fitting of directions estimation for cyclostationary signals is made. The analytic expressions of asymptotic estimation variance are derived, from which many interesting conclusions are achived, e.g, estimation variance*s relationship with the arrival angles of interference: the nearer from signal arrival angle ,the smaller the estimation deviation; and its relationship with cyclic correlation strength: the stronger ,the better the estimation. Finally, the agreement of the results expected by the theory with the computer simulation is shown.

MAA2 – Single-Rate and Multirate Filters

Chair: Charles Creusere

Naval Air Warfare Center

9:00 am – 12:30pm - ***Room: Colton II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA2-1 -- The Design of Optimum Filters for Quantizing a Class of Non Bandlimited Signals

Tuqan, Jamal, and Vaidyanathan, P.P., *California Institute of Technology*

We consider the efficient quantization of a class of non bandlimited signals, namely the class of discrete time signals that can be recovered from their decimated version. By definition, these signals are oversampled and it is reasonable to expect that we can reap the same benefits of well known efficient A/D conversion techniques. Indeed, by using appropriate multirate reconstruction schemes,we first show that we can obtain a great reduction in the quantization noise variance due to the oversampled nature of the signals. To further increase the effective quantizer resolution, noise shaping is introduced by optimizing linear time invariant (LTI) and linear periodically time varying (LPTV)M pre- and post filters around the quantizer. Closed form expressions for the optimum filters and the minimum mean squared error are derived for each case.

MAA2-2 -- M-th Band Filter Design Based on Cosine Modulation

Oraintara, Soontorn, and Nguyen, Truong Q., *Boston University*

This paper presents a design method for linear phase filter with arbitrary cutoff frequencies using cosine modulation. The approach can be applied to any existing linear phase filters with rational cutoff frequencies. Halfband filter is used to derive approximately maximally-flat filter with different cutoff frequencies, and the resulting filter can be expressed in closed form when the original filter has closed form expression. The filters satisfy M-band conditions with comparable transition band to the original filter. Simulations are presented to confirm the design method.

MAA2-3 -- An Iterative Quadratic Programming Method for Multirate Filter Design

Mo, Y.-S ; Lu, Wu-Sheng; and Antoniou, Andreas, *University of Victoria*

An iterative quadratic programming method for multirate filter design is described. The design problem is formulated as a 4th-order nonlinear optimization problem in which the objective function is a weighted sum of a reconstruction term and an aliasing-error term. Constraints on the filter's frequency response in the passband and stopband are imposed as a set of linear inequalities. the optimization problem is solved by iteratively minimizing a quadratic function subject to a set of linear constraints. Explicit formulas for evaluating the minimums of these quadratic functions are described, which lead to an efficient and fast algorithm. An example is included to illustrate the design method.

MAA2-4 -- Filter Structures of Allpass and FIR Filters for Interpolation and Decimation with Factors of Two

Johsnsson, Haken, and WanHammer, Lars, *Linkoping University*

Filter structures for interpolation and decimation with factors of two are introduced. The structures are derived by using the frequency-response masking approach, in which the overall filter is composed of a periodic model filter, its complementary periodic filter, and two masking filters. The model and complementary model filters consist of two allpass filters in parallel, whereas the masking filters are linear-phase FIR filters. In the final interpolators and decimators, the filtering takes place at the lower of the two sampling rates involved. The design of the overall filters concerns separate designs of a half-band IIR model filter and a linear-phase FIR filter. One major advantage of the new filters is that the allpass filters are functions of z2M of which results in an M-fold increase of the maximal sample frequency compared with conventional half-band IIR filters. In the case where one of the allpass branches is a pure delay, resulting in approximately linear phase, the arithmetic complexity can also be reduced. Examples are included that demonstrate this.

MAA2-5 -- Realization of General 2-D Linear-Phase FIR Filters Using Singular-Value Decomposition

Zhu, Wei-Ping, Ahmad, M. Omair, and Swamy, M.N.S., *Concordia University*

In this paper, the singular-value decomposition (SVD) technique is investigated for the realization of 2-D linear-phase FIR filters with arbitrary magnitude responses. A parallel realization structure consisting of a number of 1-D FIR filters is obtained by applying the SVD to the impulse response of a 2-D filter. By using the symmetry propertyof the 2-D impulse response and by developing an appropriate unitary transform, a singular-value decomposition yielding 1-D linear-phase constituent filters is obtained. It is shown that the number of parallel sections can be reduced significantly by neglecting the smaller singular values and allowing only a very small error in the magnitude response of the realized 2-D filter.

MAA2-6 -- New Insights Into Multirate Systems With Stochastic Inputs Using Bifrequency Analysis

Akkarakaran, Sony and Vaidyanathan P.P., *California Institute of Technology*

In multirate processing, it is often necessary to understand how the statistical properties of signals (such as stationarity) are altered by passage through multirate systems. Some of these issues have been addressed in [1]. For example, it is shown in [1] that a necessary and sufficient condition for the output of an L-fold interpolation filter to be wide sense stationary (WSS) for all WSS inputs, is that the filter have an aliasfree (L) support. However this result was established using conventional tools such as polyphase matrices, which resulted in a convoluted derivation which does not provide much insight. It also leaves many questions unanswered, since it does not generalize easily to the case of systems with vector inputs. This paper shows that problems of this nature can be addressed in an elegant and insightful manner by using bifrequency maps [2], [3], and bispectra [4]. In particular, we give a simpler proof of the above-mentioned result of [1], and generalize it to the case of vector systems.

MAA2-7 -- Synthesis of 2-D Half-Band Filters using the Frequency Response Masking Technique

Low, Seo-How, and Lim, Yong-Ching, *National University of Singapore*

Recently, the frequency response masking technique has been extended to the synthesis of sharp 2-D filters. While it has been demonstrated that sharp diamond-shaped filters may be realized efficiently, thetechniques previously presented cannot be applied to the synthesis of 2-D diamond-shaped half-band filters. In this paper, we propose a modification of the technique for the synthesis of such filters. By taking advantage of the special properties of 2-D half-band filters, the complexity of the band-edge shaping and masking filters are also reduced. This yields a very efficient implementation of the 2-D diamond-shaped half-band filter.

MAA2-8 -- Continuous-Time Signal Processing Based on Polynomial Approximation

Vesma, Jussi; Hamila, Ridha; Renfors, Markku; and Saramaki, *Tampere University of Technology*

A new approach for continuous-time processing of a discrete-time signal is proposed. This approach is based on simple modifications of the Farrow structure, which is a polynomial-based interpolation technique employing discrete-time filters for enabling arbitrary resampling of a time series. In this paper, an extension of the Farrow structure for other time-domain operations used for signal analysis than just interpolation is presented. Filter optimization and design examples corresponding to each application using the minimax optimization criterion are provided. Also, an illustrative example of the time-domain performance of this approach is given.

MAA3 – Neural Networks for Intelligent Signal Processing Special Session

Chair: Chung-Yu Wu

National Chiao Tung University

Organizers: Chung-Yu Wu

National Chiao Tung University

Fathi Salam

Michigan State University

Paul Hasler

Georgia Institute of Technology

Sponsors: Neural Systems and Applications Technical Committee

Multimedia Systems and ApplicationsTtechnical Committee

VLSI Systems and Applications Technical Committee

9:00 am – 12:30pm - ***Room: Colton III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA3-1 -- Dynamical Functional Artificial Neural Networks (D-FANNs) for Intelligent Signal Processing

de Figueiredo, Rui J.P.,*University of California, Irvine*

For the sake of clarity and precision, intelligent signal processing will be defined as the process of mapping a signal x into a binary vector y, so that y enables the detection, classification, or interpretation of an event present in x. We denote by f the input-output map of such an intelligent signal processing filter. In a number of applications it is possible to implement the nonlinear filter map f by an artificial neural network(ANN). In the present paper we consider the case in which the signal x is an analog signal (waveform) belonging to L^2(I), where I is an appropriate interval of the real line R^1, and propose the realization of f by an artificial neural network in which the synaptic weight actions of the first layer are implemented by a filter bank. We call such a network a dynamical functional artificial neural network (D-FANN) to distinguish it from a conventional functional artificial neural network (FANN), where a synaptic weight action is implemented by a scalar product in L^2(I), between the incoming waveform x and a functional weight. Thus, compared with conventional FANNs, D-FANNs permit simple and

meaningful causal realizations of intelligent analog signal processors. A novel element is the introduction of a D-FANN gain equation, in a way analogous to that in Kalman Filtering. Applications of D-FANNs to real and simulated data are now in progress and these results will be presented at the symposium (ISCAS-98).

MAA3-2 -- Voice Output Extraction by Signal Separation

Erten, G., *IC Tech*, Inc. and Salam, Fathi M., *Michigan State University*

The ability to selectively enhance audio signals of interest while suppressing spurious ones is an essential prerequisite to widespread practical use of voice activated systems. Such audio signal discrimination allows for selective amplification of a single source of speech within a mixture of two or more signals, including noise and other speakers' voices. This paper will present the most recent improvements on the algorithms we are developing, which are derived through realistic modeling of signal mixing environments in tandem with the use of dynamic multidisciplinary adaptation methods. The underlying technologies used in the compiled voice output extractor (VOX) software can significantly facilitate the embedding of speech recognition into many environments.

MAA3-3 -- Compact Neural Network Detector for Hard-Disk Drive Using Zero-Forcing Preprocessing

Wang, Michelle Y. and Sheu, Bing J., *University of Southern California*

The algorithm and architecture of a compact neural network based partial response maximum likelihood (PRML) detector with zero-forcing preprocessing for hard-disk drive reading channels are discussed. The data preprocessing technique to improve the performance and simulation result are also presented.

MAA3-4 -- VLSI Chaotic Pulse Coded Modulator Using Neural Type Cells

Sellami, Louiza, *US Naval Academy/ University of Maryland;* Zaghloul, Mona E., *The George Washington University;* and Newcomb; Robert W., *University of Maryland*

A means of modulating information signals in both additive and multiplicative ways by chaotic signals is considered. The chaotic signals are obtained from neural type cells set to their oscillation mode. The information containing signals are modulated by these chaotic signals by introducing each as the input to a differential pair. These circuits could possibly be used in communications systems for coding transmissions where the demodulation would consist of subtracting/dividing correlated signals again generated by neural type cells, as well as in neural networks based upon chaotic neurons and chaotic control of trajectories of dynamical nonlinear systems.

MAA3-5 -- A Multi-Relsolution Image Registration for Multimedia Application

Huang, Chung-Lin, and Chang, Pen-Yiing, *National Tsing-Hua University*

This paper proposes a multiresolution coarse-to-fine algorithm to align the image. By using hierarchical strategy, we can improve the execution speed and iterative convegence properties. Our algorithm is applied to align images undergoing affine, persepctieve and bilinear transformation.

MAA3-6 -- Blind Separation of Convolutive Mixtures through Parallel Stochastic Optimization

Cohen, Marc, and Cauwenberghs, Gert, *Johns Hopkins University*

We apply stochastic parallel optimization techniques to on-line blind separation of linear convolutive mixtures of independent time-varying signals. The optimization performs stochastic gradient descent on a scalar measure of statistical independence observed directly on the outputs of the unmixing network, which contains a matrix of finite impulse response (FIR) filters. We derive on-line adaptation rules, and a scalable modular architecture with minimum memory requirements amenable to parallel VLSI implementation. The architecture implements a slight modification of the network adaptation rule, which omits symmetrical non-causal terms in the computation of the stochastic gradient. Simulations indicate near-perfect separation using both versions of the rule, with a minimum phase response resulting from the simplified version.

MAA3-7 -- Recogmition of Handwritten Chinese Postal Address Using Neural Networks

Su, Yih-Ming, *I-Sheu University*; and Wang, Jhing-Fa, *National Cheng Kung University*

An automatic mail-sorting machine based on the development of a real time OCR system is proposed. The system being the first of its kind in handling Chinese mail is capable of distinguishing the city/county names in Taiwan, on handwritten/machine-printed standard Chinese style envelopes. The identification of the Chinese postal addresses is achieved by implementing an address recognition strategy that consist of a number of stages, including preprocessing, address block location, address segmentation, character recognition, contextual postprocessing, and result arbitration stages. Some empirical approaches are adopted to improve both the speed and effectiveness of postal address processing, in order to put the system to work in a real-time situation. The system architecture and related strategies are being reported. Experimental results demonstrated that the system is capable of sorting 5400 mail pieces per hour with a correct rate of 75.6% and an error rate of 0.92%.

MAA3-8 -- Intelligent Data Acquisition and Processing for Managing Higher-Education Priorities in Modern Era

Lee, Yuan Duen, *Chang Jung Christian University*; Sheu, Bing, and Young, Wayne, *University of Southern California*

Rapid Advances of microelectronics and multimedia technologies have produced significant impacts to our daily life. Computing devices have become very inexpensive and indispensable for the new generation of work force. In our study, we make first attempt to combine expertise from business and high-tech engineering to explore new solutions to challenges in the Information Age.

MAA4 – Image Processing and Coding

Chair: Ming-Ting Sun

University of Washington

9:00 am – 12:30pm - ***Room: Ferrante I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA4-1 -- A Lapped Transform Progressive Image Coder

Tran, Trac D. and Nguyen, Truong , *Boston University*

Several block-transform-based embedded image coders have been proposed recently in literature. The innovation here is to replace the wavelet transform in the EZW or SPIHT progressive image coding framework by popular block transforms such as the DCT or lapped transforms which can offer finer frequency spectrum partitioning and better energy compaction. However, most of the block transform coders above have not been able to compete with the wavelet-based ones on a consistent basis. In this paper, we present a fully progressive coding scheme based on appropriately-designed generalized lapped orthogonal/biorthogonal transforms (GenLOT or GLBT) coupled with several levels of wavelet decomposition of the DC band if needed. The uniform band block transform can be implemented in parallel fashion with fast, robust, and efficient lattice structures. Keying only on the transform stage, we are able to obtain the highest performance embedded coder up to date. This result shows that lapped transforms, when carefully designed, are capable of providing superior reconstructed image quality comparing to wavelets, both objectively and subjectively.

MAA4-2 -- Joint Channel and Source Decoding for Vector Quantized Images Using Turbo Codes

Peng, Zhishi; Huang, Yih-Fang; Costello, Daniel J.; and Stevenson, Robert L, *University of Notre Dame*

This paper presents a novel joint decoding scheme for image transmissionover noisy channels. The proposed decoding scheme includes two features of interaction between a Turbo channel decoder and a vector quantization source decoder. First, the the source decoder makes use of the channel soft outputs for better reconstruction; second, a feedback algorithm is designed for using source information to improve the error correction capability of the Turbo decoder. Significant improvement in terms of this paper presents a novel joint decoding scheme for image transmission over noisy channels. The proposed decoding scheme includes two features of interaction between a Turbo channel decoder and a vector quantization source decoder. First, the the source decoder makes use of the channel soft outputs for better reconstruction; second, a feedback algorithm is designed for using source information to improve the error correction capability of the Turbo decoder. Significant improvement in terms of the error correction capability and the quality of reconstructed images is achieved compared to a separately operating decoding system.

MAA4-3 -- An Enhanced Trellis Coded Quantization Scheme for Robust Image Transmission
Chen, Chang Wen and Li, Hongzhi, *University of Missouri-Columbia*

In this paper, we present an enhanced scheme over a trellis coded quantization (TCQ) approach recently proposed for the transmission of compressed images over noisy channels. This original scheme employs block DCT, TCQ, and fixed length bit allocation so that the compressed data is relatively insensitive to channel noise. Although the fixed length coding is able to avoid the catastrophic error propagation, one problem of the approach is the severe distortion of the whole blocks in the case of high channel error rate. To reduce the unpleasant error block effects, we propose to re-arrange the subsources of the image before the process of TCQ. With such a preprocessing, the degradation caused by the channel error can be distributed to the whole image, instead of within a particular block. Preliminary results show that this enhanced TCQ scheme is able to improve both the PSNR and the visual quality of the reconstructed image.

MAA4-4 -- Dimensional Adaptive Arithmetic Coding
Li, Weiping and Ling, Fan, *Lehigh University*

Based on conventional adaptive arithmetic coding, a Dimensional Adaptive Arithmetic Coding technique is proposed. In this technique, not only entropy coding table is generated on the fly, but also the symbol dimension is increased on the fly. Efficient and robust joint entropy coding is achieved at low complexity increase.

MAA4-5 -- An Efficient Weight Optimization Algorithm for Image Representation Using Nonorthogonal Basis Vectors
Chan, Yuk-Hee and Siu, Wan-Chi, *Hong Kong Polytechnic University*

Though image-coding techniques that employ subsets of nonorthogonal basis images chosen from two or more transform domains have been shown

consistently to yield higher image quality than those based on one transform for a fixed compression ratio, they have not been widely employed due to their very high computational complicity of existing realization approaches. This paper presents a new realization approach for mixed-transform image representation. Computational complexity can be greatly reduced compared with existing approaches.

MAA4-6 -- Morphological Signal Adaptive Median Filter for Still Image and Image Sequence Filtering

Tsekeridou, Sofia; Kotropoulos, Constantine; and Pitas, Ioannis, *Aristotle University of Thessaloniki*

A novel extension of the classical signal-adaptive median filter (SAM) is proposed in this paper, namely the morphological signal-adaptive median filter (MSAM). Three modifications are introduced in the SAM filter aiming at: (1) enhancing the SAM impulse detection mechanism so that it also detects randomly-valued impulses (2) employing an anisotropic window adaptation based on binary morphological erosions/dilations with predefined structuring sets and (3) extending its design for its application to image sequences as well. Its performance has been tested for noise suppression in both still images and image sequences. Its robustness against a wide varietyof noise distributions as well as its superiority to the classical SAM filter are proved judging from both objective (SNR, MAE) and subjective (perceived image quality) criteria.

MAA4-7 -- Vector Set Partitioning with Classified Successive Refinement VQ for Embedded Wavelet Image Coding

Mukherjee, Debargha and Mitra, Sanjit K., *University of California, Santa Barbara*.

Set Partitioning in Hierarchical Trees (SPIHT) for still image compression, proposed by Said and Pearlman, is generally regarded as a very efficient wavelet-based image compression scheme. The algorithm uses an efficient, joint scanning and bit-allocation mechanism for quantizing the scalar coefficients obtained by a wavelet decomposition of an image, and produces a perfectly embedded bitstream. In this paper, we extend set partitioning to scan vectors of wavelet coefficients, and use successive refinement VQ techniques such as multistage and tree-structured VQ to quantize several wavelet coefficients at once. The new scheme is named VSPIHT (Vector SPIHT). Some coding results are presented to demonstrate that such a vector based approach (without arithmetic coding) surpasses the scalar counterpart (also without arithmetic coding), in the mean-squared-error sense, for most images at low bitrates. The superiority of the vector-based approach is more pronounced for images that are generally regarded as difficult to code (such as Barbara) because of a large amount of detail.

MAA4-8 -- Perceptual Image Compression with Wavelet Transform

Lai,Yung-Kai and Kuo, C.C.J., *University of Southern California*

A perceptual image compression method by using the wavelet transform is proposed in this work. This method is different from conventional wavelet coding schemes by incorporating Human Visual System (HVS) characteristics in the quantization stage. Instead of encoding amplitudes of wavelet coefficients directly, we investigate the coding of contrasts of each resolution. The resulting compression scheme is able to distribute visual errors uniformly over the whole image. Thus, the visual artifact at low bit rate is minimized. Experimental results are given to show the superior visual performance of the new method in comparison with those of the conventional wavelet coders.

MAA5 – Signal Processing for Communications I

Chair: Alex Kot

Technological University

9:00 am – 12:30pm -	***Room: Ferrante II***
10:30 am – 11:00am –	*Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA5-1 -- FFT-Based Clipper Receiver for Fast Frequency-Hopping Spread-Spectrum System

Teh, K. C.; Kot, Alex C.; and Li, K.H., *Nanyang Technological University, Singapore*

This paper presents the performance analysis of a binary frequency-shift keying fast frequency-hopping spread-spectrum (BFSK/FFH SS) system equipped with a fast Fourier transform (FFT) processor and a clipper. The FFT-based clipper receiver provides an alternative approach to suppress partial-band jamming (PBJ) in discrete-time domain. The analytical expression for the probability of bit error is obtained and numerical results show that the performance of FFT-based receiver is better than that of the linear-combining receiver and comparable to that of the clipper receiver.

MAA5-2 -- Harmonic and Intermodulation due to Requantization of Fixed-Point Numbers

Hentschel, Tim and Fettweis, Gerhard, *Dresden University of Technology*

In this paper the basic equations for evaluating the power of harmonic and intermodulation distortions due to requantization (rounding or truncation) of fixed-point numbers are derived. In contrast to the papers of Abuelma'atti and Blachman we show that not only odd harmonics and intermodulation products but also even ones are produced. Special emphasis is given to the analysis of the DC error introduced by two's complement rounding. Finally we suggest some ways to circumvent this DC error.

MAA5-3 -- A Comparison of CAP/QAM Architectures

Abdolhamid, Amir and Johns, David A., *University of Toronto*

Recently CAP modulation (Carrierless Amplitude and Phase modulation) has been of wide interest to industry because of its simplicity, bandwidth efficiency and zero dc component. This paper compares CAP versus QAM modulation and highlights some practical implementation issues. In addition, three different CAP-like architectures are compared according to A/D sampling-rates, A/D resolutions and jitter requirements.

MAA5-4 -- Quantization for Robust Sequential M-ary Signal Detection

Chandramouli, Rajarathnam and Ranganathan, Nagarajan, *University of South Florida*

In this paper, a M-ary sequential detector based on the quantized received signal samples is proposed and analyzed for amplitude-modulated signals. The problem is modeled as M-ary hypothesis testing. A L level optimal quantization algorithm based on the quantiles of the received signal is presented. The proposed quantizer detector is robust to the changes in the channel parameters. For an average decision error probability equal to 10^{-4}, 4.6 dB of transmitted signal power is saved by using the proposed quantizer detector when compared to the fixed sample size detector.

MAA5-5 -- The Optimal RLS Parameter Tracking Algorithm for a Power Amplifier Feed-Forward Linearizer

Chen, Jiunn-Tsair; Tsai, Huan-Shong; and Chen, Young-Kai, *Stanford University*

Digital signal processing (DSP) techniques have been proposed in recent years to adaptively track the control parameters of a power amplifier (PA) feed-forward linearizer. In most of the propositions, gradient-based searching algorithms are applied to the parameter tracking. In this paper, we propose an optimal RLS (recursive least square) parameter tracking algorithm, which significantly accelerates the convergence speed and eliminates the gradient noise. There exists two problems for the RLS algorithm. First, the least square solution is not the optimal solution because of the nonlinearity of the PA. Second, the vector modulator (VM) which introduces the control parameters into the linearizer circuit may not be accurate enough to provide a precise power gain and phase shift calculated by the DSP. We solve both problems, respectively, by rearranging the circuit components and by constraining the VM characteristics. We also present simulation results to verify the performance improvement of the proposed algorithm.

MAA5-6 -- Selectivity and Sensitivity Performances of Superregenerative Receivers

Vouilloz, Alexandre and Declercq, M., *Swiss Federal Institute of Technology*

This paper is dedicated to an in-depth analysis of superregenerative receivers performances. A preliminary study of start-up time and steady-state amplitude of the oscillator signal is first achieved. Then analytical relations are established and discussed for the selectivity and sensitivity of superregenerative receivers in different modes of operation.

MAA5-7 -- A New Model for the DOA Estimation of the Coherent Signals
Jin, Liang; Li, Jiang, and Yin, Qinye, *Xi'an Jiaotong University*

Based on the movement of the sources, a new model for the DOA estimation of the coherent signals is proposed herein, under which the signals and their multipath counterparts are decorrelated without spatial smoothing or spatial signature estimation, and the cyclic methods such as cyclic MUSIC and cyclic ESPRIT can be directly employed in the multipath scenarios, so that the signal selectivity and interference suppression can be achieved in practical mobile communication. The effectiveness of this new model is demonstrated by simulation results.

MAA5-8 -- A System Scheme for Downlink Selective Beamforming In Smart Antenna
Jin, Liang, Li, Jiang, and Yin, Qinye, *Xi'an Jiaotong University*

In this paper the generalized equivalent feed model is established for downlink multiple beamforming in FDMA/FDD system with multiple users sharing the same channel. Based on this model, a system scheme is proposed for MSK modulation, where the digital beamforming and channel allocation can be accomplished at base band, which means the possibility of using DSP and software radio technology.

MAA6 – Low-Power IC Techniques

Chair: Eby G. Freidman

University of Rochester

9:00 am – 12:30pm -	***Room: Ferrante III***
10:30 am – 11:00am –	*Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA6-1 -- Signal Coding for Low Power: Fundamental Limits and Practical Realizations
Ramprasad, Sumant; Shanbhag, Naresh R.; and Hajj, Ibrahim N., *University of Illinois at Urbana-Champaign*

Transitions on high capacitance busses in VLSI systems result in considerable system power dissipation. Therefore, various coding schemes have been proposed in the literature to encode the input signal in order to reduce the number of transitions. In this paper we derive achievable lower and upper bounds on the expected signal transition activity. These bounds are derived via an information-theoretic approach in which symbols generated by a source (possibly correlated) with entropy rate H are coded with an average of R bits/symbol. These results are applied to, 1.) determine the activity reducing efficiency of different coding algorithms such as Entropy coding, Transition coding, and Bus-Invert coding, 2.) bound the error in entropy-based power estimation schemes, and 3.) determine the lower-bound on the power-delay product. Two examples are provided where transition activity within 4% and 8%

of the lower bound is achieved when blocks of 8 and 13 symbols respectively are coded at a time.

MAA6-2 -- Finite-State Machine Partitioning for Low Power

Benini, Luca and Giovanni, De Micheli, *Stanford University*; and Vermeulen, Frederik, *IMEC*

We describe an algorithm for the automatic synthesis of a network of interacting FSMs starting from a single state-table specification. The sub-machines in the decomposed FSM communicate through a set of additional interface signals. The decomposed implementation has low power dissipation because one single sub-machine is clocked at any given time and it controls the outputs values while all other sub-machines are idle. There is full cycle-by-cycle equivalence between the input-output behavior of the decomposed and undecomposed implementation.

MAA6-3 -- Use of Charge Sharing to Reduce Energy Consumption in Wide Fan-in Gates

Khellah, Muhammad M., and Elmasry, Mohamed I., U*niversity of Waterloo, Canada*

This paper presents a novel technique to reduce the energy and delay of dynamic large fan-in gates. The basic idea is to generate a low swing output signal by first charging a small dummy capacitor and then discharging it on the (pre-discharged) gate output. By employing the principle of charge sharing, a small swing will be created on the gate output. This swing can be then detected and restored to CMOS level using a sense amplifier. Simulation results illustrates 2-4 times energy savings and up to 3.6 times speed-up as compared to conventional dynamic approaches. The design of a 32x32 TLB in a 0.6 um process using the proposed approach is also described.

MAA6-4 -- Low Power/Low Swing Domino CMOS Logic

Rjoub, Abdoul and Koufopavlou, Odysseas, *University of Patras*; and Nikolaides, S.,*University of Thessaloniki*

A new low-power domino CMOS logic is introduced. Its power characteristics are based on a low voltage swing technique. The output inverter of the domino gate is modified in order to reduce its output voltage swing. This results in dynamic power dissipation saving up to 36% and improvement in the power-delay product. A technique for creating changeable values of the voltage swing is used achieving various trade-off between power savings and speed. Experimental results clearly show the validity of the proposed technique for low-power operation.

MAA6-5 -- Power Optimization of Combinational Modules Using Self-Timed Precomputation

Mota, Antonio S. and Monteiro, Jose C.,*IST-INESC*; Oliveira, Arlindo L., *Cadence Europ0ean Labs/IST-INESC*

Precomputation has recently been proposed as a very effective power management technique. Precomputation works by preventing some of the inputs from being loaded into the input registers, thus significantly reducing the switching activity in the circuit. In this paper, we present a self-timed approach for the precomputation of combinational logic circuits. This technique allows for maximum power savings without the need of a clock signal. However, we may incur in some delay penalty. We describe how to achieve significant power reductions without increasing the maximum delay, by choosing a judicious placement of the latches in the combinational logic circuit. Experimental results are presented for arithmetic modules, confirming that power dissipation can be

greatly reduced with marginal increases in circuit area and almost zero delay increase.

MAA6-6 -- A Mathematical Approach to a Low Power FFT Architecture

Stevens, Kenneth S., *Intel* and Suter, Bruce, *Rome Labs, US Air Force*

Architecture and circuit design are the two most effective means of reducing power in CMOS VLSI. Mathematical manipulations have been applied to create a power efficient architecture of an FFT. This architecture has been implemented in asynchronous circuit technology that achieves significant power reduction over other FFT architectures. Multirate signal processing concepts are applied to the FFT to localize communication and remove the need for globally shared results in the FFT computation. A novel architecture is produced from the polyphase components that is mapped to an asynchronous implementation. The asynchronous design continues the localization of communication and can be designed using standard cell libraries such as radiation-tolerant libraries for space electronics. We present a methodology based on multirate signal processing techniques and asynchronous design style that supports significant reduction in power over conventional design practices. A test chip implementing part of this design has been fabricated and power comparisons have been made.

MAA6-7 -- A Configurable 32nd Order Low Voltage Low Power Digital Filter for Portable Communications Systems

Suvakovic, Dusan and Salama, C. Andre T., *University of Toronto*

A low power 32nd order digital filter for portable audio applications has been designed and implemented in a single threshold 1V, 0.5um CMOS process. The design is full custom, using a combination of conventional CMOS and pass transistor circuits, optimized for low energy consumption and small area. The filter features up to 16 biquad sections with programmable coefficients and performs fixed point computations with 16-bit resolution. The measured average energy consumption of 330pJ per biquad computation indicates that the implementation of complex DSP in a single threshold low voltage process is a viable alternative for implementations in multiple threshold processes.

MAA6-8 -- Optimal Design of Low Power Nested Gm-C Compensation Amplifiers Using a Current-based MOS Transistor Model

Xie, X.; Schneider, M.C.; Embabi, S.H.K.; and Sanchez-Sinencio, Edgar, T*exas A&M University*

A sound design of low power multistage amplifiers is presented. The amplifiers are stabilized by Nested Transconductance-Capacitance Compensation (NGCC).The key for an optimal design is a current-based MOSFET transistor model, which allows the amplifiers to be designed in moderate inversion. With 2V supply voltage and 10 kohm/20 pF load, a four-stage amplifier implemented in a 1.2 um n-well CMOS process achieved 1.03 MHz gain bandwidth product, 103 dB open loop gain and 62.7 phase margin with a power consumption of 0.3 mW. The active area of the amplifier is 0.0052 mm2. With the same specifications, a three-

stage amplifier was also integrated in the 1.2 um n-well CMOS process. Compared to the design in strong inversion, both amplifiers satisfy the specifications while the power consumption is reduced by a factor of 3.

MAA7 – Chaos and Applications

Chair: Martin Hasler

Swiss Federal Institute of Technology Lausanne

9:00 am – 12:30pm -	***Room: Bonzai I***
10:30 am – 11:00am –	*Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA7-1 -- Synchronous Phenomena from Chaotic Circuits with Intermittently Coupled Capacitors
Takanori, Matsushita; Saito, T.; and Torikai, H., *Hosei University*

This paper proposes intermittently coupled capacitors (ab. ICC) in order to consider synchronous phenomena of chaotic circuits. We have clarified theoretically that this system exhibits chaos synchronization, synchronization of periodic attractor and co-existence of them. Some of these phenomena are demonstrated in the laboratory.

MAA7-2 -- BER Performance of a Chaos Communication System Including Modulation-Demodulation Circuits
Wada, Masahiro, *Tokushima University*; Kawata, Junji, *Tokushima Bunri University*; Nishio, Yoshifumi; and Ushida, Akio, *Tokushima University*

In this article, estimation of bit error rate (BER) performance in a general chaos communication system in cluding modulation-demodulation circuits is investigated. We observe influences of modulation-demodulation circuits by both computer simulation and SPICE simulation. BER is calculated by computer simulation. We confirm that nonlinearity of modulation-demodulation and several circuits influence chaos synchronization and also communication quality.

MAA7-3 -- Chaos Shift Keying in the Presence of Noise: A Simple Discrete Time Example
Hasler, Martin, *Swiss Federal Institute of Technology Lausanne*

The transmission of binary information using chaotic switching, also called chaos shift keying is used. On the receiver side the information is extracted using a method that is not based on synchronization, but that directly tries to detect which chaotic system of the two can have produced the received signal, provided the channel noise is bounded by a known value. The results obtained are not yet as good as for conventional systems, but they constitute a step forward in the performance of transmission systems based on chaos. The more traditional decoding method based on chaos synchronization is aso analyzed, and if used in an efficient way, also gives quite good results.

MAA7-4 -- Chaotic Signals for CW-Ranging Systems - a Baseband System Model for Distance and Bearing Estimation
Bauer, Andreas, *Technical University of Dresden*

In this paper the application of chaotic signals in ranging systems is addressed. In [NORSIG'96] the idea of using chaotic signals as ranging signals in continuous wave (CW) systems has been introduced and motivated. Possible benefits where also analysed. This paper describes realisation and signal processing problems in chaos based range and bearing estimation. All the signal processing is performed in the baseband. In order to do this an actuator/sensor pair is introduced, that matches the measurement channel to the baseband signal processing. The channel adaption of this actuator/sensor pair is a linear operation and thus allows signal processing based on the assumption of linear channel properties. An array of such sensors is formed in order to allow bearing estimation of the impinging signal.

MAA7-5 -- Design of Infinite Chaotic Polyphase Sequences with Perfect Correlation Properties

Abel, Andreas; and Goetz, Marco, *Technical University of Dresden*

In this paper we consider chaotic discrete-time systems which generate polyphase sequences. First we give the definition of infinite polyphase sequences with perfect correlation properties. Then a simple design rule for chaotic generators is derived which guarantees that the generated sequences are perfect. Following this rule we construct families of generators of infinite polyphase sequences. Finally, as an important characteristic for several applications, an explicit expression for the variance of a finite-length correlation estimator is derived.

MAA7-6 -- Design of Nonlinear Observers for Hyperchaos Synchronization Using a Scaler Signal

Grassi, Giuseppe, *Universita di Lecce*; and Mascolo, Saverio, *Politecnico di Bari*

In this paper hyperchaos synchronization is restated as a nonlinear observer design issue. This approach leads to a systematic tool, which guarantees the synchronization of a wide class of hyperchaotic systems via a scaler signal. The proposed technique has been applied to synchronize two well-known examples of hyperchaotic dynamics: Rossler's system and Matsumoto-Chua-Kobayashi circuit.

MAA7-7 -- Synchronization in Arrays of Chaotic Circuits Coupled via Hypergraphs: Static and Dynamic Coupling

Wu, Chai Wah, *IBM*

When an array of circuits is coupled via coupling elements which connects two circuits at a time, the underlying coupling topology can be represented as a graph. When the coupling element connects more than two circuits at a time, the underlying coupling topology can be represented as a hypergraph. In this paper, we study the synchronization properties in arrays of chaotic circuits where the underlying coupling topology is a hypergraph. We consider the case where the coupling is due to memoryless (static) components, and the case where the coupling is due to dynamic circuit components. We introduce the algebraic connectivity of a hypergraph and show how it can be used to derive sufficient conditions for synchronization.

MAA7-8 -- Chaotic and Bifurcation Behavior in an Autonomous Flip-Flop Circuit Used by Piecewise Linear Diodes

Okazaki, Hideaki, G*ifu National College of Technology*; Nakano, Hideo,*Shonan Institute of Technology*; and Kawase, Takehiko, *Waseda University*

A circuit realization of an autonomous flip-flop circuit used by piecewise linear tunnel diodes, producing chaotic and bifurcation behavior, are proposed. The proposed circuit is made of four linear passive element (2 capacitors, 1 inductor, 1 resistor), one active element (1 DC battery) and two piecewise linear characteristic nonlinear resistors realized by using an operational amplifier. Typical global behavior in the circuit are illustrated. By using an analysis of the one-dimensional Poincare map constructed from experimental data, chaotic behavior are examined, and the Liapunov exponents are estimated. The experimental observations are compared with the digital computer simulations.

MAA8 – Data Converters

Chair: William Black

Iowa State University

9:00 am – 12:30pm - ***Room: Bonzai II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA8-1 -- Fast Pipelined A/D Converter in CMOS Technology

Park, Sangbeom,*Texas Instruments*

In this paper, a new 8-bit pipelined A/D converter which has been fabricated in n-well CMOS technology is introduced. Even though a fully differential op-amp is preferred to obtain a high power supply rejection ratio, a single-ended op-amp is implemented in the A/D converter to investigate the speed performance of the new pipelined A/D converter. The main purpose of this work is to compare the conventional pipelined A/D converter with the new one in terms of speed. According to experiments, the new pipelined converter improves the speed by a factor of 2.5 compared to conventional pipelined A/D converters because it uses more parallel schemes. With the architecture, one can build fast low-power A/D converters in CMOS technology.

MAA8-3 -- A 200 MHz 6-bit Folding and Interpolating ADC in 0.5-um CMOS

Jiang, Xicheng; Wang, Yunti; and Willson, Jr., Alan N., *UCLA,*

This paper presents the detailed design of a 200 MHz CMOS ADC with a folding and interpolating architecture. To overcome the input-frequency-multiplication problem inherent in such architectures, a front-end Sample/Hold circuit is used. The fully differential signal is folded by a factor of five and followed by a four-times interpolation. A double-averaging technique is explored and, with this technique, the analog folding stage can achieve approximately 12-bit linearity. To suppress the misalignment error, a bit alignment circuit is designed. The prototype chip includes about 1400 components and the active chip area is 0.4

mm/sup 2/. Its power consumption is approximately 150 mW at a 200 MHz sampling rate.

MAA8-4 -- A CMOS Current-Mode Pipeline ADC Using Zero-Voltage Sampling Technique
Luong, Howard Cam and Hui, Ronny C. C., *Hong Kong University of Science and Technology*

A low-voltage low-power CMOS current-mode pipeline ADC is presented. Zero-voltage sampling technique and regulated cascode circuits are combined in the sample-and-hold circuits to increase the resolution. Dynamic latched-type comparators are used to implement high-speed low-power sub-ADCs. The multiplying DAC and the comparators are used with a digital error correction (DEC) circuit to realize a low-voltage low-power current-mode pipeline ADC. Simulation shows that the ADC can work at 20MHz with an 8-bit resolution. The power consumption is 22mW.

MAA8-5 -- A Comparison of Monolithic Background Calibration in Two Time-Interleaved Analog-to-Digital Converters
Dyer, Kenneth, *University of California at Davis*

Two background calibration methods for time-interleaved pipelined analog-to-digital converters are described and compared. One approach uses an extra ADC channel and analog calibration circuits; the other uses extra resolution and digital calibration circuits. Both approaches have been integrated in a 1-um CMOS process. The strengths and weaknesses of the two approaches are presented, and the measured data are compared.

MAA8-6 -- Improving the Linearity in High-Speed Analog-to-Digital Converters
Gatti, Umberto, *Italtel S.p.A.*

Future telecommunication systems will require A/D converters with resolution as high as 12 bit and very high linearity (>90 dB) at more than 40 MHz sampling rate. These specifications make essential the use of digital calibration for attenuating the errors due to analog components inaccuracies. In this paper we propose a correction technique suitable for off-line and on-line operation. For the first approach we use statistical methods and digital look-up tables. For the second one we suggest a system where the input signal is doubly converted: at the required speed and at a reduced rate but with an higher precision. The slow representation updates the calibration digital look-up table while the data of the fast one are corrected by the look-up table itself. Simulations using Matlab on acquired data and extensive system studies indicate more than 15 dB of improvement in the converter linearity.

MAA8-7 -- On the Dynamic Performance of High-Speed ADC Architectures
Gustavsson, Mikael, *Linkoping University*, and Tan, Nianxiong, *Microelectronics Research Center*

For wideband radio and high-speed internet access applications the ADC is a crucial building block and a high SNDR over a wide signal band is required.

However, most publications on ADCs have not focused on improving the dynamic range at high signal frequencies and they do not meet the requirements for wideband radio and high-speed internet access applications. This paper presents a tutorial discussion on high-speed CMOS ADCs concerning the dynamic performance and points out some fundamental limitations of different architectures in order to achieve high dynamic performance over a wide signal band.

MAA8-8 -- Modelling of CMOS Digital-to-Analog Convertors for Telecommunication
Wikner, J. Jacob, *Linkoping University*, and Tan, Nianxiong, *MERC, Ericsson Components AB*

In telecommunication applications the digital-to-analog convertor is a crucial building block. For this kind of applications dynamic performance, rather than static performance, is of the greatest importance. This paper discusses the aspects of the dynamic performance of digital-to-analog convertors and models the influence of nonideal components (such as output impedance, mismatch, circuit noise, etc.) on the dynamic performance. The purpose of this modelling is to provide an insightful design guidance for high dynamic performance digital-to-analog convertors.

MAA9 – Symbolic Analysis Methods and Their Applications to Analog Circuit Design

Chair: Marwan Hassoun
Iowa State University

Organizers: Marwan Hassoun **Special Session**

Iowa State University

Lawrence Huelsman

Arizona State University

9:00 am – 12:30pm - ***Room: Bonzai III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA9-1 -- Applications of Symbolic Methods to Circuit Design: An Overview
Konczylowska, Agnieska, *Laboratoratoire de Bagneux*; Hassoun, Marwan M., *Iowa State University*; Huelsman, Lawrence, *University of Arizona*

This paper presents an overview of the popular applications of symbolic methods nowadays as they pertain to circuit design. The specific applications that are discussed are: insight into circuit behavior, device modeling and extraction, behavioral and functional modeling and structural synthesis. The

application of symbolic analysis in each of these areas is illustrated via a description of a specific methodology.

MAA9-2 -- Exploring Data Conversion Architectures by Symbolic Computation

Horta, Nuno Cavaco Gomes, *Universidade Nova de Lisboa*; and Franca, Jose E., *Instituto Superior Tecnico*

The implementation of an algorithm-driven methodology for the synthesis and characterization of data converter systems, using extensively symbolic methods, is described. The synthesis process is, here, started at the algorithm-level allowing an unconstrained specification of a broad range of conversion systems, when compared to the traditional architecture oriented design tools. More, the exploration of new architectures and their characterization at the sub-block level, is performed fully automatically.

MAA9-3 -- A Symbolic Approach for Testability Evaluation in Fault Diagnosis of Nonlinear Analog Circuits

Fedi, Giulio; Giomi, Riccardo; Manetti, Stefano, and Piccirilli; Maria Cristina, *University of Florence*

A symbolic approach for testability evaluation in fault diagnosis of nonlinear analog circuits is presented. The new approach extends the methodologies developed for the linear case to circuits where nonlinear components, such as diodes or transistors, are present. The testability evaluation is a fundamental information for the fault diagnosis process, whatever method will be used, also in the nonlinear case. An example of circuit verifying this consideration and the validity of the proposed approach is briefly presented.

MAA9-4 -- Symbolic Analysis Of Microwave Circuits

Benboudjema, Kamel, *COM DEV Space Group*; Boukadoum, M. *Universite du Quebec a Montreal*; Vasilescu, G. and Alquie,G., *LEAM, Universite Pierre et Marie Curie*

The polynomial interpolation (PI) method is one of the most suitable symbolic analysis techniques for the computation of linear transfer functions when the only circuit variable is the complex frequency p. In this article, we present improvements to the PI method so that it may be used for the computation of network functions in a fully symbolic form, using only numerical algorithms. We provide examples of how to use the new approach to directly determine the microwave performances, such as the scattering parameters, of given networks.

MAA9-5 -- Behavioral Modeling of PWL Analog Circuits Using Symbolic Analysis

Fernandez, Francisco V.; Perez-Verdu, Belen; and Rodriguez-Vazquez, Angel, *Instituto de Microelectronica de Sevilla*

Behavioral models are used both for top-down design and for bottom-up verification. During top-down design, models are created that reflect the nominal behavior of the different analog functions, as well as the constraints imposed by

the parasitics. In this scenario, the availability of symbolic modeling expressions enable designers to get insight on the circuits, and reduces the computational cost of design space exploration. During bottom-up verification, models are created that capture the topological and constitutive equations of the underlying devices into behavioral descriptions. In this scenario symbolic analysis is useful because it enables to automatically obtain these descriptions in the form of equations. This paper includes an example to illustrate the use of symbolic analysis for top-down design.

MAA9-6 -- Efficient Statistical Analog IC Design Using Symbolic Methods

Debyser, Geert; Leyn, F.; Gielen, Georges; and Sansen, W., *Katholieke Universiteit Leuven ESAT-MICAS*; and Styblinski, M., *Texas A&M University*

A new statistical design methodology is presented that uses symbolic methods to increase the efficiency of statistical IC design. The methodology is implemented in an environment that combines the symbolic design equation manipulation engine DONALD with the generic statistical design system GOSSIP.DONALD is used to generate the initial design and to create the symbolic computational plan that is used by GOSSIP for the actual statistical yield, Cp and Cpk optimization.The strengths and weaknesses of the proposed approach are discussed, and its accuracy and speed are compared with the traditional method of using a SPICE-type circuit simulator in the inner loop of the statistical optimization. Overall, a significant speed-up of the statistical IC design efficiency is observed.

MAA9-7 -- Approximate Symbolic Pole/Zero Extraction Using Equation-Based Simplification Driven by Eigenvalue Shift Prediction

Henning, Eckhard; Sommer, Ralf; and Wiese, Michael, *Institut fuer Techno- und Wirtschaftsmathematik*

This paper presents a new approach to symbolic pole/zero analysis of linear electronic circuits using equation-based simplification techniques driven by novel term ranking and error control strategies. Term rankings are determined by using a linear prediction formula to estimate the shifts of the eigenvalues of interest caused by removing terms from a matrix equation. The shift estimations are based on one initial solution of a numerical generalized eigenvalue problem. Error control is achieved by tracking the true eigenvalue shifts numerically. The algorithm allows for the computation of approximated symbolic expressions for selected poles and zeros, including non-dominant ones.

MAA9-8 -- Efficient Symbolic Analysis of Large Analog Circuits Using Sensitivity-Driven Ranking of Matroid Intersections

Dobrovolny, Petr, *Technical University Brno*; Wambacq, Piet; Gielen, Georges; and Sansen, Willy, *Katholieke Universiteit Leuvan*

A new program for the generation of approximate symbolic network functions is presented. The approximation technique used in this tool is the simplification during expression generation technique, which in the general case suffers from a nonpolynomial CPU complexity. The technique makes use of the two-graph method. Using matroid intersection theory, spanning trees common to the voltage and the current graph are directly generated at selected sample frequencies. The generation of the approximate symbolic expression of a network function is driven by the sensitivity of the magnitude of the network function with respect to the different coefficients. In this way, very little terms are generated more than once. The total algorithm runs in O(Kmn^3) time. Here, K is

the average number of matroid intersections that must be generated for the approximation of each coefficient of the network function, n is the number of nodes in the linearized network and m is the number of circuit elements. Experimental results are presented and a comparison to previous methods based on matroid intersection theory is given.

MAA10 – Low Power Digital Circuit Design

Chair: Naresh Shanbhag

University of Illinois

9:00 am – 12:30pm - ***Room: San Carlos I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA10-1 -- Analytical Expressions for Average Bit Statistics of Signal Lines in DSP Architectures

Bobba, Sudhakar; Hajj, Ibrahim N.; and Shanbhag, Naresh R., *University of Illinois at Urbana-Champaign*

Accurate high-level power estimation methods are required for exploring the design space to obtain an optimal low-power circuit. DSP architectures are regular and they consist of interconnected macro-blocks such as adders and multipliers. In [1], the power dissipation of macro-blocks was related to the average bit statistics. Given the input word-level statistics for a DSP architecture, the word-level statistics at all the internal signal lines can be computed analytically using transfer function evaluation or by propagating the statistics. In this paper, we present simple analytical expressions for computing the average bit statistics using the word-level statistics of the signal lines in a DSP architecture.

MAA10-2 -- Architecture Selection of a Flexible DSP Core Using Reconfigurable System Software

Lee, Jong-Yeol; Lee, Dae-Hyun; Kim, Jong-Sun; Yoon, Hyun-Dhong; Kyung, Chong-Min; Park, Kyu-Ho; Lee, Yong-Hoon; and Hwan, Seung H., *Korea Advanced Institute of Science and Technology*

MetaCore is a flexible DSP core in that the architecture of MetaCore can be modified easily by changing the hardware parameters. To fully exploit the merits of a flexible core, the system software must be re-configurable when the target architecture changes. In this paper, we present a re-configurable system software for a flexible DSP core and the architecture selection procedure called "compile-simulate-refine" cycle using the re-configurable system software. The "compile-simulate-refine" cycle can make it possible to select the best architecture for a given application by exploring the possible candidate architectures in short time.

MAA10-3 -- Analyzing Effects of Cache Parameters on Memory Power Consumption Of Video Applications

Kapoor, Bhanu, *Texas Instruments Incorporated*

Energy effcient computing is growing in demand as portable systems require energy effciency in order to maximize the battery life. We provide data and insight into how the choice of cache parameters affects memory power consumption of video algorithms. We make use of memory traces generated as a result of running typical video algorithms to simulate a large number of cache configurations. The cache simulation data is then combined with on-chip and off-chip memory power models to compute memory power consumption. The configurations of particular interest are the ones that optimize power under certain constraints. We also study the role of process technology in these experiments. In particular, we look at how moving to a more advanced process technology for the on-chip cache affects optimal points of operation with respect to memory power consumption.

MAA10-4 -- Transformational-Based Synthesis Of VLSI Based DSP Systems for Low Power Using A Genetic Algorithm

Bright, Marc Stephen and Arslan, T., *Cardiff University Of Wales*

This paper describes a technique for the synthesis of CMOS based DSP systems under multiple design constraints. The primary target of the technique is to reduce operating power by applying high level transformations to designs. During the search for a low power solution the technique considers issues at circuit and layout levels, using appropriate capacitive models, together with tracking speed and area design constraints. In exploring the complex search space of the synthesis problem the technique uses a Genetic Algorithm which utilizes a library of high level transformation based techniques within its operators. The paper describes the technique, the capacitive models used for power estimation and presents results for DSP systems of varying complexity. The results demonstrate the significant power savings achieved with the technique.

MAA10-5 -- Power Estimation Using Input/Output Transition Analysis (IOTA)

Lucke, Lori E.; Lee, Junsoo; and Vinnakota, Bapi, *University of Minnesota*

Optimizing power dissipation is now a major concern in IC design. Accurate power estimation at the circuit level is too expensive. Tools which estimate power dissipation at higher levels of abstraction without sacrificing accuracy are of interest. We discuss a new cell-library based technique for power estimation. An IO transition model is developed to represent energy consumption in library elements. Power estimation based on the IO model requires less computational effort than with previous models. The IO model also addresses a accuracy limitation of previous models. A power estimation tool IOTA, based on this model, has been implemented in C and Matlab. For reasonably large combinational and sequential arithmetic circuits, IOTA has an average error of 5% and low simulation time compared to SPICE simulations.

MAA10-6 -- Fast Delay-Dependent Power Estimation of Large Combinational Circuits

Jou, Jer Min, *National Cheng Kung University*; Chen, Shung-Chih, *Nan-Tai Institute of Technology*; and Wang, Chih-Liang, *National Cheng Kung University*

In this paper, we propose a fast and memory-efficient algorithm to estimate the glitch effects of the circuit under a general delay model without constructing global BDDs and without calculating Boolean difference. A new concept, where the circuit's signal activities with and without glitching effects are separately calculated by two newly developed calculation modules, is developed. The combined Markov chain and BAM method is used, and approximates the transient signals behavior with the steady state behavior, then the glitching effects as well as the temporal and spatial correlations among signals are all considered and processed efficiently. The analysis of our method indicates that it is applicable to large size circuits with acceptable errors.

MAA10-7 -- Resynthesis of Sequential Circuits for Low Power

Roy, Sumit, *Ambit Design Systems;*and Banerjee, Prithviraj, *Northwestern University*

At the logic level, a popular approach is to power down the sequential machine during the self-loops of the underlying finite state machine(FSM). In this work, we extend this idea to resynthesize existing sequential circuits to reduce power. We report a novel technique based on symbolic simulation of a sequential circuit to extract its self-loops without extracting the corresponding state transition diagram(STG). Since self loops may not be inherently present in the corresponding FSM, we partition the circuit heuristically and identify partial-self-loops for each partition to bring down the corresponding sub-circuit by gating the clock sub-tree feeding that partition. By using this approach, we could save

upto 45% of the total power on a controller circuit of a microprocessor design, where traditional techniques could not save any power.

MAA10-8 -- STG Optimization for Power and Area Reduction
Panagiotaras, George, S. and Koufopavlou, Odysseas G. *University of Patras*

Graph transformations for deterministic Signal Transition Graphs (STGs) are presented. The proposed transformations can result in more efficient circuits with respect to power consumption and area, by reducing the STG signals concurrency, provided that the timing restrictions of the circuit are not violated. The circuits' function and speed are preserved. The proposed graph modifications steps are presented in a procedural, clearly defined algorithm. So the transformations can be very easily integrated in existed STG synthesis tools.

MAA11 – VLSI Circuits for Multimedia Signal Processing

Chair: Magdy Bayoumi

University of Southwestern Louisiana

9:00 am – 12:30pm - ***Room: San Carlos II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA11-1 -- A Paradigm for Collaboration across a Globally Networked Environment: Implementation of ISCAS '98 Internet Services
Coffman, James W. and McEachen, John, *Naval Postgraduate School*

Using current internet technology, an interactive and automated system can be developed to replace traditional aspects of professional and scientific conference organization - particularly those related to receiving, processing, distributing, reviewing and scheduling papers submitted for conference presentations. A two-stage prototype was developed and used for the 1998 IEEE International Symposium on Circuits and Systems (ISCAS '98) to demonstrate and evaluate the effectiveness of this methodology. The initial prototype was used to collect and process the preliminary extended summaries, as well as facilitate the review and scheduling processes. A follow-on prototype was developed for the final camera-ready submissions based on evaluation results of the initial prototype. A comparison of both prototypes and an analysis of their effectiveness is presented.

MAA11-3 -- A Flexible MPEG Audio Decoder Layer III Chip Architecture
Singh, P., Moreno, W., Ranganathan, N. and Neinhaus, H.,*University of South Florida*

Moving Pictures Expert Group (MPEG) audio Layer III is the most advanced standard for digital audio compression. The high coding gain of the standard is due to its time to frequency mapping section, which is also the most compute

intensive part of the audio coder. It has been shown in the literature that the Discrete Cosine Transform (DCT) proposed in the standard for the filterbank section could be implemented using the Fast Hartley Transform (FHT) in order to reduce the amount of computations and memory accesses. In this paper, an efficient approach is proposed for implementing the synthesis filter bank of the MPEG audio Layer III. The approach is based on a mixed radix FHT ofr implementing the Inverse Modified Discrete Cosine Transform (IMDCT) section and a radix-2 FHT for the subband decoding section. A high throughput pipeline VLSI architecture is designed for implementing the proposed approach. The architecture has been simulated and verified using the Cadence Verilog-XL simulator.

MAA11-4 -- Low Power 2D DCT Chip Design For Wireless Multimedia Terminals

Chen, Liang-Gee, Jiu, Juing-Ying, Chang, Hao-Chieh, Lee, Yung-Pin and Ku, Chung-Wei, *National Taiwan University*

In this paper, a low power 2-D DCT architecture based on direct 2-D approach is proposed. The direct 2-D consideration reduces computational complexity. According to this algorithm, a parallel distributed arithmetic (DA) architecture at reduced supply voltage is derived. In the real circuit implementation of the ship, and adder of low power consumption is designed, as well as a power-saving ROM and a low voltage two-port SRAM with sequential access. The resultant 2-D DCT ship is realized by 0.6mm single-poly double-metal technology. Critical path simulation indicates a maximum input rate of 133MHz, and it consumes 138mW at 100MHz.

MAA11-5 -- Influences of Object Based Segmentation onto Multimedia Hardware Architectures

Ohmacht, Martin, Wittenburg, Jens-Peter and Pirsch, Peter, *University of Hannover*

This paper describes essential differences in the video coding part of recent multimedia communication schemes (as the MPEG-4 standard being currently under development) to conventional schemes (as MPEG-1, MPEG-2 or ITU H.26x) caused by the possibility to work on arbitrarily shaped objects rather than only on rigid square blocks of pels. Methods employing parallel ways of operation are presented for maintaining high data throughput caused by the real time constraints of video communication schemes. Object based segmentation significantly increases the hardware costs to exploit the parallelization resources inherent with the employed algorithms. The paper compares the efficiency of recent multimedia hardware architectures when operating on object based schemes under real time constraints and proposes architectural measures to increase efficiency and performance in these cases.

MAA11-6 -- New Video And Multimedia Standards And Their Impact To Implementation

Chen, Tsuhan, *Carnegie Mellon University*

In the development of video and multimedia standards, new algorithms often result from the need to improve the efficiency or to reduce the cost of implementation. On the other hand, new implementation techniques are often triggered by algorithms that are too computation intensive with existing technology. Therefore, in multimedia applications, the development of algorithms and the progress in architectures are closely tied to each other. In

this paper, we will introduce a number of new video and multimedia standards and discuss special implementation considerations demanded by these new standards.

MAA11-7 -- Providing Multicast Video on Demand using Native-mode Asynchronous Transfer Mode
Lockwood, John W.; Kang, Sung Mo; Hossain, Ashfaq; and Hiltenbrant, John, *University of Illinois*

A network video server and client devices have been designed and prototyped that use multicast to deliver Motion-JPEG, MPEG-1, and MPEG-2 video on top of IP, IP-over-ATM and native-mode ATM (AAL5) protocols. The server runs on a workstation-class machine, while the clients have been implemented both as a multi-threaded software entity and as a stand-alone ATM network-attached playback device. Scalability of the video distribution network is obtained by using multicast features of the underlying network. Feedback from the clients and a single video frame retransmission mechanism are used to decrease end-to-end frame loss.

MAA11-8 -- 3-D Discrete Wavelet Transform Architectures
Weeks, Michael and Bayoumi, Magdy, *University of Southwestern Louisiana*

Compression is a significant operation in many 3-D data applications, such as Magnetic Resonance Imaging (MRI), Medical Diagnosis, Television, and Seismic Data. Employing standard 2-D compression techniques do not offer efficient solutions in these applications. In this paper, a 3-D Discrete Wavelet Transform (DWT) approach is proposed for performing 3-D compression. Two architectures are presented. The first architecture, called 3D-I, is a straight-forward implementation of the 3-D DWT. It allows even distribution of the processing load onto 3 sets of filters, with each set doing the calculations for one dimension. The filters are easily scalable to a larger size. The control for this design is very simple, since the data are operated on in a row-column-slice fashion. The design is cascadable. Due to pipelining, all filters are utilized 100% of the time, except for the start up and wind-down times. The second proposed architecture, 3D-II, uses block inputs to reduce the amount of on-chip memory. It has a control unit to select which coefficients to pass on to the low and high pass filters. The RAM on the chip is small compared to the input size, since it depends solely on the filter sizes. The filters are parallel, since systolic filters assume that the data is fed in a non-block form such that partial calculations are done.

MAA12 – VLSI Digital Circuits

Chair: Yvon Savaria

Ecole Polytechnique Montreal

9:00 am – 12:30pm -	***Room: San Carlos III***
10:30 am – 11:00am –	*Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA12-1 -- Design of Low Power Differential Logic Using Adiabatic Switching Technique
Lo, Chun-Keung and Chan, Philip C.H., *The Hong Kong University of Science and Technology*

This paper presents a new adiabatic circuit technique called adiabatic differential cascode voltage switch with complementary pass-transistor logic tree (ADCPL). Power reduction is achieved by recovering the energy in the recover phase of the supply clock. Energy dissipation comparison with other logic circuits is performed. Simulation shows that for a pipelined ADCPL carry look ahead adder, a power reduction of 50% to 70% can be achieved over static CMOS case within a practical operation frequency range.

MAA12-2 -- Ultra Low-Voltage Digital Floating-Gate UVMOS (FGUVMOS) Circuits
Berg, Yngvar; Wisland, Dag T.; Lande, Tor Sverre; and Mikkelsen, Sindre, U*niversity of Olso*

This paper describes a novel technique for implementing ultra low-voltage/low-power digital circuits. The threshold and supply voltage can be set to desired values while exposing the chip to UV-light. UV-light activated conductances between the power supply rails and the floating gates are used to program the desired threshold shift in any standard double poly CMOS process. Measured characteristic of a programmed inverter is shown.

MAA12-3 -- Single Ended Swing Restoring Pass Transistor Cells for Logic Synthesis and Optimization
Pihl, Johnny, *Royal Military Institute of Technology*

In this contribution we present three cells in pass transistor logic which can be directly appended to any CMOS standard cell library, and provide improvements in timing, power and area. These cells utilize N-type pass transistor logic and single ended swing restoration as opposed to the dual rail swing restoration in SRPL[3]. The three cells are 2-input exor, 2-input multiplexer and 4-input multiplexer. Circuit simulations indicate an overall delay improvement on all timing arcs compared to traditional CMOS implementations, and in benchmark tests for logic optimization, delay and power were improved by up to 29% and 36%, respectively.

MAA12-4 -- Edge Reversal-Based Asynchronous Timing Synthesis
Franca, Felipe Maia Galvao; Alves, Vladimir Castro; and Granja, Edson do Prado, *COPPE/UFRJ*

A synthesis methodology for the production of self-timed versions of digital circuits designed under the synchronous approach is introduced. The methodology is based on Scheduling by Edge Reversal (SER), a very simple and powerful distributed synchronizer. Its correctness is proved and it is shown how, as a result of applying it to a given target (synchronous) circuit, a functionally equivalent asynchronous SER-driven circuit is produced.

MAA12-5 -- A New True-Single-Phase-Clocking (TSPC) BiCMOS Dynamic Pipelined Logic

Tseng, Yuh-Kuang and Wu, Chung-Yu, *National Chiao-Tung University*

New true-single-phase-clocking BiCMOS dynamic logic circuits and BiCMOS Dynamic latch logic circuits for high-speed dynamic pipelined system applications are proposed and analyzed. The circuit performance of the new BiCMOS cynamic logic circuits and BiCMOS dynamic latch logic circuits are simulated by using HSPICE in 1 mm BiCMOS technology. Simulation results have shown that the operating frequency of the pipelined system which is constructed by the new dynamic latch logic circuits, is 204.1 MHz under 1.5 pF output loading at 2.3V. It is 2.86 times of the operating frequency in the CMOS TSPC dynamic pipelined system.

MAA12-6 -- Low Voltage BiCMOS TSPC Latch for High Performance Digital Systems
Nikolic, Borivoje, *University of California* and Oklobdzija, Vojin G., *Integration/UC-Davis*

New true single-phase clock (TSPC) BiCMOS circuits are described. The TSPC latches are intended for use in high-performance deeply pipelined digital electronic systems. The circuits described are based on quasi-complementary BiCMOS circuit using single-phase clock. They are verified to have full-swing operation with supply voltages as low as 1.5V. The speed and power performance of the new latch is superior to previously published results, which was confirmed by simulation in 0.5um technology.

MAA12-7 -- Low Ringing I/O Buffer Design
Carro, Luigi and Bego, Lauro Jardim, *Universidade Federal do Rio Grande do Sul*

This paper describes the design of a new I/O buffer architecture, allowing low ringing at the presence of inductive package noise. A simple and accurate model of the I/O buffer can be used to help semi-custom users foresee pad behavior under different load and inductive packaging situations. Analysis results and simulations of the behavioral model were validated by a discrete prototype. The new buffer design reached higher frequencies without noise degradation when compared with traditional buffer design.

MAA12-8 -- CMOS Circuit Design of Threshold Gates with Hysteresis
Sobelman, Gerald E. and Fant, Karl, *Theseus Logic, Inc.*

M-of-N threshold gates with hysteresis form a class of circuit elements that have important application in NULL Convention Logic(TM), a novel asynchronous logic design methodology. General design guidelines for these M-of-N gates are presented using CMOS technology. Three types of circuit implementations are discussed: static, semi-static and dynamic. In addition, initialization techniques are presented for use in establishing a known initial state.

MAA13 – Communications Circuits Poster Session

Chair: Robert H. Caverly

Villanova University

9:00 am – 12:30pm - ***Room: Serra Ballroom Back I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA13-1 -- Nonlinear Properties of Gallium Arsenide and Silicon FET-Based RF and Microwave Switches

Caverly, Robert H, *Villanova University*

An important parameter for RF and microwave system design is the prediction of distortion produced by system components. This paper presents the results of a study on modeling the distortion produced by silicon and gallium arsenide RF and microwave switches. Exact relationships for the second and third order intercept point as a function of FET parameters are presented. The results indicate that both types of FET-based switches have higher levels of distortion at low frequencies. The distortion improves at frequencies above the gate bias circuit cutoff frequency, although the distortion improvement is lower for the MOSFET-based switch.

MAA13-2 -- A 3-V 45-mW CMOS Differential Bandpass Amplifier for GSM Receivers

Leung, David Lap Chi and Luong, Howard Cam, *Hong Kong University of Science & Technology*

A 3V CMOS differential bandpass amplifier to be integrated in a GSM RF front-end is presented. With a center frequency tuning circuit, the center frequency can be varied from 877 to 962MHz, and with a Q-compensation circuit, the Q-value can be tuned from 3 to 230. Detailed analysis of the noise figure including the resistive losses in on-chip inductors is given. With a 3V supply and a Q of 32, the amplifier achieves a noise figure of 5.2dB, a power gain of 25dB and consumes 45mW. The IIP3 and Po-1dB are -32.5dBm and -44dBm respectively.

MAA13-3 -- Gb/s Encoder/Decoder Circuits for Fiber Optical links in Si-Bipolar Technology

Mokhtari, Mehran; Ellervee, Peter; Schuppar, Gerd; Juhola, Tarja; and Tenhunen, Hannu, *Royal Intitute of Technology*

Encoder/Decoder circuits operational up to 1.3 Gb/s have been realized in Si-bipolar technology. The current consumption is 95mA resp. 125 mA at 4.3V. The structures utilize new architectures, to our knowledge, never published before. The circuits are aimed for applications in parallel fiber optical communication links to achieve true DC-coupled transmission.

MAA13-4 -- A Comparative Analysis of CMOS Low Noise Amplifiers for RF Applications

Mayaram, Kartikeya and Ge, Yongmin, *Washington State University*

Four CMOS RF low noise amplifier (LNA) circuits have been analyzed. These analyses include the effect of induced gate noise for the MOSFET. The noise factor contribution from each noise source is derived and these circuits are then compared for a minimum noise factor. The MOSIS HP 0.35um and 0.8um CMOS technologies have been used for performance comparisons. An automatic synthesis system for LNA design is also described.

MAA13-5 -- The Characterization of Micromachined CMOS Transmission Lines for RF Communications

Ozgur, Mehmet, Milanovic, Veljko, Zincke, Christian and Zaghloul, Mona E., *The George Washington University*

This work reports on the analytical and experimental characterization of micromachined microwave transmission lines used in RF communication applications. New analytic approximations are derived for the quasi-static capacitance of coplanar transmission lines with finite metalization thickness. The expressions are well suited for CAD applications since they are compact and scalable. Furthermore, their accuracy is comparable with the fabrication tolerances and measurement accuracy achievable.

MAA13-6 -- A 2.0-GHz Submicron CMOS LNA and a Downconversion Mixer

Litmanen, Petteri Matti, *Texas Instruments*; Ikalainen, P.and Halonen, Kari A., *Helsinki University of Technology*

A 2-GHz 'all transistor' LNA and a downconversion mixer have been implemented with a standard digital 0.5-um CMOS process. The LNA has been measured to have a noise figure of 5.4 dB and a 8.3-dB gain at 2.0 GHz. The Gilbert-type downconversion mixer with a 0-dB conversion gain to a differential 100-ohm load and DSB noise figure of 11 dB has been measured. These processed circuits demonstrate the capability of submicron CMOS technology for high frequency applications.

MAA13-7 -- Easy Simulation and Design of On-Chip Inductors in Standard CMOS Processes

Christensen, Kåre Tais and Jergensen, Allan, T*echnical University of Denmark*

This paper presents an approach to CMOS inductor modelling, that allow easy simulation in SPICE-like simulators. A number of test results are presented concerning optimal center hole, inductor area, wire spacing and self-inductance. Finally a comprehensive design guide is provided on how to design close-to-optimal inductors without the use of electromagnetic simulators.

MAA13-8 -- Programmable Low Noise Amplifier with Active-Inductor Load

Zhuo, Wei, Pineda de Gyvez, Jose and Sanchez-Sinencio, Edgar, *Texas A&M University*

A common gate CMOS low noise amplifier(LNA) with an active-inductor load is presented. For large inductance values, an on-chip passive inductor requires considerable silicon area and it is quality-factor (Q) limited; a situation that can be rended as impractical. Hence, the purpose of this work is to seek the possibility of using active inductors in RF circuits as substitutes for passive ones. Moreover, an active inductor opens avenues for programmability, e.g. it is possible to attain an amplifier with a programmable center frequency. It is shown in this paper that by proper design optimization the active-inductor's noise contribution can be minimized. HSPICE simulations using 0.5um HP technology show that our amplifier has a tuning range of half decade for a center frequency

at 1 GHz. The simulated gain, noise figure, and power consumption are 20dB, 3.65dB and 14mw, respectively.

MAA13-9 -- Electro-Mechanical Properties of a Micromachined Varactor with a Wide Tuning Range
Dec, Aleksander M.and Suyama, Ken, *Columbia University*

This paper discusses the electro-mechanical properties of a new micromachined varactor structure that can achieve a wide tuning range. An experimental device was fabricated in a polysilicon surface micromachining process. The varactor achieves a tuning range of 40 percent and a quality factor of 9.75 at 1 GHz when the capacitance is set to 3.62 pF.

MAA13-10 -- A Low Voltage Design Technique For Low Noise RF Integrated Circuits
Abou-Allam, Eyad and Manku, Tajinder, *University of Waterloo*

Analysis and optimization of the bias conditions and noise parameters of MOS devices are presented. A design technique based on a narrowband LC-folded cascode topology is proposed for low voltage RF integrated Circuits. The technique is applied to the design of a 1V LNA operating at 1.9 GHz using a 0.5 um CMOS technology. Simulation results show that the LNA provide a noise figure of 1.7 dB, gain of 10 dB, and is well matched at the input. The LNA also provides a minimum noise figure of 1.6 dB.

MAA13-11 -- A 1.8GHz CMOS Quadrature Voltage-Controlled Oscillator (VCO) Using the Constant-Current LC Ring Oscillator Structure
Wu, Chung-Yu and Kao, Hong-Sing, *National Chiao Tung University*

A new fully integrated CMOS quadrature voltage-controlled oscillator (VCO) realized in a standard 0.5mm double poly double metal (DPDM) CMOS technology is proposed, that combines a fully differential two-stage ring oscillator with LC tanks and negative resistance to provide both inphase and quadrature output signals. The phase noise is low due to the use of the resonator-type oscillator. The simulation results show that with an on-chip varactor tuned resonator and a control voltage of 0-3 V, the tuning range of the VCO is 160MHz from 1.67GHz to 1.83GHz. Under 1% mismatch of the inductor or capacitor, the phase error of VCO outputs are less than 1° from perfect quadrature and the amplitude ratio are less than 1.0007. The power dissipation is 35mW for 3V power supply. The area is 1.3x0.9 mm2, dominated by the two integrated spiral inductors.

MAA13-12 -- Low Voltage, 2 X 2, 25 Gb/s Crosspoint Switch in InP-HBT Technology
Mokhtari, Mehran, *Royal Institute of Technology*

An asynchronous 2 X 2 crosspoint switch in InP-HBT technology has been designed fabricated and characterized. BER-measurements at 20 Gb/s show no erroneous transmission. The eye-diagram at 25 Gb/s is clearly open. The circuit is operational at 2V supply voltage, with a current consumption of 120 mA,

including the 50 ohm drivers. To the best of our knowledge, This circuit has the lowest power consumption at low operation voltage at 25 Gb/s.

MAA13-13 -- A CORDIC-Based Digital Quadrature Mixer : Comparison with a ROM-Based Architecture

Nahm, Seunghyeon, Han, Kyungtae and Sung, Wonyong, *Seoul National University*

This paper describes a CORDIC-based digital quadrature mixer in comparison with a ROM-based architecture. This architecture employs the circular rotation mode of the CORDIC algorithm for signal mixing as well as carrier generation, while the ROM-based architecture requires an additional complex multiplier for signal mixing. To optimize the hardware design parameters, the finite word-length effects of two implementation architectures are analyzed numerically. In addition, the simulation-based word-length determination is also conducted for the application to QPSK and QAM demodulators. The hardware costs of them are estimated, which shows that the CORDIC-based architecture occupies only a third of the area of the ROM-based architecture.

MAA13-14 -- Reconfigurable Signal Processing ASIC Architecture for High Speed Data Communications

Grayver, Eugene, *UCLA*

A flexible and reconfigurable signal processing ASIC architecture has been developed, simulated and synthesized. The proposed architecture can be used to realize any one of several functional blocks needed for the physical layer implementation of high speed data communication systems operating at symbol rates over 60 Msamples/sec. In fact, multiple instances of a chip based on this architecture each operating in a different mode can be used to realize the entire physical layer of high speed data communication systems. The architecture features the following modes (functions): real and complex FIR/IIR filtering, least mean square (LMS) based adaptive filtering, Discrete Fourier Transforms (DFT), and direct digital frequency synthesis (DDFS) at up to 60Msamples/sec. All of the modes are mapped onto a common, regular datapath with minimal configuration logic and routing. Multiple chips operating in the same mode can be cascaded to allow for larger blocks

MAA13-15 -- Dual Loop DSP-PLL with Wide Frequency Acquisition Range and Fast Frequency Acquisition

Obote, Shigeki, *Tottori University*; Sumi, Yasuaki, *Tottori Sanyo Electric Co. Ltd.*; Syoubu, Kouichi, Fukui, Yutaka and Itoh, Yoshio, *Tottori University*

In this paper, we propose a new Dual Loop Digital Signal Processing type Phase Locked Loop (Dual Loop DSP-PLL) using Digital Signal Processing type Frequency Locked Loop (DSP-FLL) which we propose and the first order TAN type DSP-PLL (TAN-DSP-PLL). It is confirmed by the simulation results that Dual Loop DSP-PLL can pull in the frequency without cycle slip up to half of the sampling frequency. Moreover, the frequency acquisition time is faster and

phase variance is smaller than those of the second order TAN-DSP-PLL. Therefore, the performance of the proposed Dual Loop DSP-PLL is superior to conventional DSP-PLLs.

MAA13-16 -- Pipelined Arrays for Modular Multiplication

Ciminiera, Luigi, *Politecnico di Torino*

New arrays performing the modular multiplication are presented; they operate on a bit-serial basis for both inputs and outputs. The distinctive characteristic of the arrays presented is the possibility to start a new operation, as soon as the cells in the array are no longer used for the previous one, thus allowing bit-level pipelining of the different multiplications. A first array presented has a short clock cycle and long latency, so that it is more suited for applications dealing with long blocks of data to be processed. A second one has a longer clock cycle and shorter latency, and it is more suited for repeated operation on the same block of data.

MAA13-17 -- Distortion and Noise Performance of Bottom-Plate Sampling Mixers

Yu, Wei , and Leung, Bosco, *University of Waterloo*

Distortion and noise in a bottom-plate sampling mixer are analyzed. The method of Volterra series is used to analyze distortion. The effects of continuous time, time varying, and sampling distortions are considered. Frequency domain method is used to analyze thermal noise. The method of stochastic differential equation is used to solve for LO noise. These two noise effects, when combined with LO jitter, give a complete noise picture. The analysis is performed in sampled data domain. Explicit formulas are given to guide the design of bottom-plate sampling mixers.

MAA13-18 -- A Digital Frequency Modulator Circuit for a Dual-Mode Cellular Telephone

Lahti, Jukka A. and Niemistö, Matti, *University of Oulu*

An all digital frequency modulator circuit architecture for a dual-mode cellular telephone is described. The aim in the design of the circuit has been to find out the advantages in terms of power consumption that can be obtained with a hardware realization of the modulator as compared to a software solution based on a commercial DSP chip. The results show that the power consumption can be reduced significantly with moderate silicon area.

MAA13-19 -- Design of a 2.4 GHz CMOS Frequency-Hopped RF Transmitter IC

Kosunen, Marko, Vankka, Jouko, Waltari, Mikko, Sumanen, Lauri, Koli, Kimmo, and Halonen, Kari, *Helsinki University of Technology*

A 2.4 GHz frequency-hopped RF transmitter IC has been designed and implemented in a 0.5 um CMOS. This frequency hopped spread spectrum (FH/SS) transmitter is intended for use in a wide variety of indoor/outdoor portable wireless applications in the 2.4-2.4835 GHz ISM frequency band. The transmitter

***is capable of frequency and phase modulation. The key elements in the* transmitter are: a quadrature direct digital synthesixer, digital-to-analog converters, low-pass filters, upconversion mixers and 90 degrees phase splitter.**

MAA13-20 -- A Bipolar Semi-Custom PLL-Based Synthesizer for GSM and DCS Systems

Hakkinen, Juha Tapio; Rahkonen, Timo; and Kostamovaara, Juha, *University of Oulu*

A versatile synthesizer chip capable of operating with an output signal of up to 2 GHz and a reference signal of up to 20 MHz was designed in MAXIM's GST-2 Process using QuickChip-9-60D transistor array. The circuit includes the basic building blocks of a complete PLL-based synthesizer except for the VCO and the loop filter. The chip has an internal dual modulus prescaler operating in 8/9 or 16/17 mode. The circuit has a 10 bit M counter and a 4 bit pulse swallow counter and a phase-frequency detector. The level of the PFD output can be set externally from 0.5 mA to 5.0 mA. Depending on the PFD output level, the circuit uses from 90 mA to 122 mA from a 5 V supply. The differences between the full custom and semi-custom design processes are discussed and attention is paid to the minimization of device usage.

MAA13-21 -- Adaptive FEC on a ReConfigurable Processor for Wireless Multimedia Communications

Arrigo, Jeanette F., Page, Kevin J., Wang , Yuhe and Chau, Paul M., *University of California San Diego*

Due to variations in environmental conditions, many computationally intensive algorithms that need to be processed in a compact form factor often require a more flexible solution than a specialized ASIC. A ReConfigurable Processor Board (RCP) was jointly developed by the University of California San Diego and L3 Communications Corporation for implementing Digital Signal Processing (DSP) algorithms for wireless multimedia communications. The flexible architecture of the RCP makes it ideal for performing parallel tasks and can process multiple algorithms concurrently. As an application example, an Adaptive Viterbi Decoder (AVD) was designed and implemented on the RCP. The AVD can adapt itself to varying channel characteristics and service requirements at run time. It is capable of processing data with constraint lengths from 7 to 15 and code rates from 1/2 to 1/6. The AVD provides robust decoding for video, audio and data communication channels.

MAA13-22 -- Low-Power, Low-Phase-Noise CMOS Voltage-Controlled-Oscillator with Integrated LC Resonator

Park, Byeong-Ha and Allen, Phillip E., *Georgia Institute of Technology*

Integrated low-power, low-phase-noise voltage-controlled-oscillator (VCOs) have been designed using a 0.5um CMOS technology with three metal layers. The achieved phase noise is as low as -110dBc/Hz at an offset frequency of 200KHz, at a power consumption of only 6.6mW with a 3.3V power supply. The tuning range is as large as 14%.

MAA13-23 -- PLL Frequency Synthesizer with Multi-Programmable Divider

Sumi, Y., Syoubu, K., Obote, S., and Fukui,. Y., *Tottori University*

The lock-up time of a PLL frequency synthesizer depends on each loop gain. In this paper, we pay attention to the gain of a programmable divider which is one of the important elements of PLL, and propose a new method for improving the gain of programmable divider. In order to achieve the increase in gain of the programmable divider, we propose a new PLL frequency synthesizer with multi-programmable divider by which the gain is increased even when the same reference frequency and the same division ratio as usual are used. It will be shown by the theoretical considerations and experimental results that a higher speed lock-up time can be achieved.

MAA13-24 -- A 3.3V 600Mhz - 1.30Ghz CMOS Phase-Locked Loop for Clock Synchronization of Optical Chip-to-Chip Interconnects

Sheen, Robin R.-B. and Chen, Oscal T.-C., *National Chung Cheng University*

A high-speed phase-locked loop for clock synchronization of optical chip-to-chip interconnects has been developed. It consists of a photo-diode, an amplifier, a phase detector, a charge pump, a loop filter, and a voltage control oscillator. In order to make our phase-locked loop operate in optical interconnects efficiently, we apply an improved fully integrated CMOS photo-detector, and propose a new phase-locked loop with a high-speed three-state phase detector and a wide-range voltage control resistor. The proposed phase-locked loop has been implemented by using the UMC 0.5um CMOS technology with a die size of 300um5400um. The HSPICE simulation results show that the optical signals from 1.2Gb/s (600MHz) to 2.6Gb/s (1.3GHz) can be locked at a supply voltage of 3.3V. The jitter of proposed phase-locked loop at 1GHz is less than 15ps. Its power consumption is around 150mW. Therefore, our phase-locked can be widely used in high-frequency and low-power optical chip-to-chip interconnect systems.

MAA14 – Circuits and Power Systems Poster Session

Chair: Graham R. Hellestrand

University of New South Wales, Australia

9:00 am – 12:30pm - ***Room: Serra Ballroom Back II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA14-1 -- Amplitude Bounds on Oscillations from a Sigma-Delta Modulator Structure

Davies, Anthony C., *King's College London*

Sufficient conditions are given for the zero-input non-linear oscillations of a SD modulator containing a 3rd order digital-filter to be bounded to a specified cube in the state-space. These oscillations have an adverse effect upon performance

in many applications,so knowledge of amplitude bounds may be of practical significance. Short-period oscillations give rise to narrowband spectral 'tones' which are typically more objectionable than the spectral content of long-period oscillations so conversion of oscillations from short-period into longer period can be useful. Some discussion is included of the effect of a deterministic 'bit flipping' method for breaking up short period oscillations on the amplitude bounds.

MAA14-2 -- Global Synchronization in Coupled Map Lattices

Wu, Chai Wah, *IBM*

This paper presents a global synchronization theorem for coupled map lattices. Roughly speaking the theorem states that the coupled map lattice x_n+1 = AF(x_n) synchronizes if A has an eigenvalue 1 of multiplicity 1 corresponding to the synchronization manifold and the other eigenvalues of A are close to zero. Examples of coupled map lattices of logistic maps are used to illustrate the result. In particular, we give global results regarding synchronization in coupled map lattices for which previously only numerical evidence and local results were available. We show that (1) globally coupled maps synchronize if the coupling is large enough, (2) randomly coupled maps are synchronized if the number of couplings for each map is large enough and (3) coupled maps connected on a graph will synchronize if the ratio between the largest and the smallest nonzero eigenvalue of the Laplacian matrix of the graph is small.

MAA14-3 -- On-off Intermittency from a Ring of Four Coupled PLLs

Hasegawa, Akio; Igarashi, Ryo; Endo, Tetsuro, *Meiji University*; and Komuro, Motomasa, *Teikyo University of Science & Technology*

This paper investigates on-off intermittency from a ring of four coupled PLLs. We find some parameter values at which on-off intermittency occurs by calculating the transversal Lyapunov exponent, and demonstrate on-off intermittency both by computer simulation and electronic circuit experiment. From some facts, we elucidate that the intermittency observed at these parameter values is really on-off intermittency. Moreover, we clarify the generation mechanism of on-off intermittency geometrically by investigating bifurcations of the periodic orbits in the invariant manifold.

MAA14-4 -- Performance Comparison of Communication Systems Using Chaos Synchronization

Kawata, Junji, *Tokushima Bunri University*; Nishio, Yoshifumi, *Tokushima University*; Dedieu, Herve, *Swiss Federal Institute of Technology*, and Ushida, Akio, *Tokushima University*

In this article, the performance of some communication systems using chaos synchronization is evaluated and compared. The evaluation of bit error rate is done for not ideal communication channel but lossy and noisy one. It is confirmed that a chaos-based communication system has a good performance which may be almost the same compared with conventional analog modulation schemes.

MAA14-5 -- Synchronization in Chaotic Oscillators Based on Classical Oscillator Coupled by One Resistor

Sekiya, Hiroo; and Moro, Seiichiro, *Keio University*; Mori, Shinsaku, *Nippon Institute of Technology*; and Sasase, Iwao, *Keio University*

We propose the system of the simple chaotic oscillators which are based on Wien-bridge oscillator coupled by one resistor and investigate synchronization in the proposed system. Further, we propose the system of the simple chaotic oscillators which are based on van der Pol oscillator coupled by one resistor. In the system of chaotic oscillators which are based on Wien-bridge oscillator, N-phase synchronization cannot be observed but in-phase and anti-phase synchronization can be observed regardless of N. In synchronization of chaos, these synchronization phenomena are first observations as far as we know. In case of the system of chaotic oscillators which are based on vander Pol oscillator, N-phase synchronization can be observed. From the results, it is said that the synchronization of the classical oscillators and that of the chaotic oscillators based on them have common characteristics when classical oscillator is Wien-bridge oscillator or van der Pol oscillator.

MAA14-6 -- Neural-Network Based Adaptive Control of Uncertain Chaotic Systems

Qin, Huashu and Zhang, Huaizhou, *Chinese Academy of Science*; and Chen, Guanrong, *University of Houston*

In this paper, a new adaptive control scheme, that employs a Gaussian radial basis function network with output weights updated on-line, is developed for regulating a class of uncertain chaotic systems. Theoretical analysis guarantees that the controlled uncertain chaotic systems can asymptotically track target orbits within arbitrarily small tolerance bounds. The uncertain Duffing-Holmes system is used as an example for illustration.

MAA14-8 -- Time Domain Analysis of Modulated Carriers in (Non)-Linear Systems

Leenaerts, Domine, *Technical University Eindhoven*

A technique will be proposed to separate carrier and modulated signals from modulated carriers in linear or nonlinear systems. The method gives insight in amplitude and phase behavior of the modulated signal in the time domain and allows faster computation.

MAA14-9 -- Singularities of Implicit Ordinary Differential Equations

Reißig, Gunther, *Technische University Dresden*; Boche, Holger, *Heinrich-Hertz-Institut fuer Nachrichtentechnik Berlin*

This paper concerns quasi-linear implicit differential equations of form 0=A_1(x)x'- g_1(x), 0=g_2(x), where A_1:U->L(R^n,R^{n-m}) and g_1:U->R^{n-m} are of class C^1, g_2:U->R^m is of class C^2, U is an open subset of R^n, n,m are natural numbers, m<n. In particular, the above differential equation is considered about impasse points x_0 in U, i.e., points x_0 beyond which solutions are not continuable. Under appropriate assumptions, it is shown that there is a diffeomorphism that transforms solutions of the above implicit differential equation near such points into solutions of the normal form x_1^r x_1' = sigma, x_2' = 0, ..., x_{n-m}' = 0, x_{n-m+1}=0, ..., x_n=0 near 0, and vice versa, where sigma=+/-1=const. In particular, standard impasse points in the sense of Rabier and Rheinboldt lead to the above normal form with r=1. A practical example for r=2 is also given.

MAA14-10 -- Useful Necessary and Sufficient Condition for Reachability of Extended Marked Graphs

Tsuji, Kohkichi, *Aichi Prefectural University*

In this paper, by using the state equation of a Petri net, we derive a necessary and sufficient condition for reachability of extended marked graphs (EMGs). In particular, these conditions can be checked easily because they are presented in

terms of the initial token distribution, the final token distribution, and its net structure. Furthermore, by using this necessary and sufficient condition, we can derive also the necessary and sufficient condition for a behavioral trap in EMGs.

MAA14-11 -- Calculation of the Homoclinic Bifurcation Sets of PLL Equation with Five-Segment Piecewise-Linear Phase Detector Characteristic

Ohno, Wataru; and Endo, Tetsuro, *Meiji University*

It is well-known that phase-locked loops (PLLs) can generate chaos. Many types of PLLs have been studied,because the theoretical results agree well with the experimental results in practical circuit. Melnikov's method enables us to calculate a parameter region for the transversal homoclinic points in many types of PLL equations with small damping. But, it is not easy to calculate this parameter region for practical PLL systems with large damping. We computed the parameter region for a second-order PLL with sinusoidal and symmetric triangular phase detector (PD) for small damping case via Melnikov's method analytically. In we computed it for large damping case by calculating the Melnikov's integral numerically. We computed it analytically for large damping case for PLLs with symmetric and asymmetric triangular PD, using the nature of piecewise linear vector field, and succeeded in obtaining results with small numerical errors. Based on the above previous studies, we will calculate the homoclinic bifurcation curves for a second-order large-damping PLL with five segment piecewise linear PD via Melnikov's method. We confirm the validity of the bifurcation curves by drawing the stable and unstable invariant curves at the predicted parameter values. Finally, we clarify that the extinction mechanism of the running chaotic attractor can be explained by the collision with the stable invariant curve, which is called the `Blue Sky Catastrophe'.

MAA14-12 -- Algorithm for Non-Intrusive Identification of Residential Appliances

Cole, Agnim I. and Albicki, Alexander, *University of Rochester*

An algorithm has been developed to use at a central processing site for identifying appliances and appliance usage at remotely monitored residences. This algorithm is part of a non-intrusive system that uses sampled data for real and reactive power accumulated over an extended period of time. Using a logic analysis, the algorithm can recognize at least six major appliances, including a heat pump, as well as any two appliances that turn on or off at nearly the same time. Data from several residences in the Rochester, NY, and Columbus, OH, areas have been analyzed during this study.

MAA14-13 -- The Resolution of Algebraic Loops in the Simulation of Finite-Inertia Power Systems

Ciezki, John G.; and Ashton, R.W., *Naval Postgraduate School*

The move toward incorporating more-electric technology into naval combatant shipboard power systems and the requisite analysis of such systems have driven the development of accurate detailed simulation strategies for stiffly-

connected, finite-inertia networks. Since typical bus loads including electric machines are described by voltage-in current-out models, the resultant algebraic loop must be resolved by either inserting artificial components into the network or by reformulating the component models. The authors introduce an alternative algebraic solver approach that obviates the need for developing complex nonstandard component representations and eliminates the tradeoff between speed and accuracy inherent to the artificial component approach. Using a standard simulation package and a representative portion of a shipboard power system, the authors then contrast their approach with two methods commonly reported on in the literature.

MAA14-14 -- On Stability Robustness of Discrete-Time Systems: The Complex-Variable Approach of Mastorakis

Lu, Wu-Sheng, *University of Victoria*

The key element of Mastorakis' approach is the well-known theorem of Rouche: Suppose f(z) and d(z) are analytic in domain D and on its simple closed boundary, and suppose that |d(z)| < |f(z)| on the boundary. Then f(z) and f(z)+d(z) have the same number of of zeros in D. By taking the nominal and perturbed denominator polynomials of a stable discrete-time transfer function as f(z) and f(z)+d(z) respectively, and taking the unit disk as D, Rouche's theorem is directly connected to a stability-robustness study. This paper proposes an enhanced complex-variable approach initiated by Mastorakis to derive several improved bounds for stable coefficient perturbations of a nominal Schur polynomial.

MAA14-15 -- Phase-Jitter Dynamics of Second-Order Digital Phase-Locked Loops

Rogers, Alan; Teplinsky, Alexey; and Feely, Orla, *University College Dublin*

Recent studies of digital phase-locked loops by Gardner have shown that an unwanted phase 'jitter' occurs in such systems, due to frequency quantisation in a number-controlled oscillator. In a previous paper, we used techniques from the theory of nonlinear dynamics to verify Gardner's empirical results and to illuminate the behaviour of first- and second-order loops. In this paper we shall expand on that work; in particular, we shall consider both the transient and steady-state dynamic behaviour of the second-order DPLL and describe mathematically the motion of steady-state trajectories when the input frequency is rational.

MAA14-16 -- Analysis of the DC Link Current Spectrum in Force Commutated Inverters

Mariscotti, A., *University of Genoa*

A general expression for the spectrum of the dc-link current of three-phase Voltage Source Inverters is derived for load unbalances, defining positive, negative and zero sequence components. Several inverter modulations are then considered and the corresponding properties of the dc-ling current are analyzed.

MAA14-17 -- On the Modeling of a Chaotic Circuit Containing a Bent Hysteresis Resistor

Xia, Cheng-Quan, *Xian Jiaotong University*; and Du, Min, *Trident Microsystems, Inc.*

This paper discuss the modeling of a third order nonlinear circuit containing a resistor with so-called bent hysteresis characteristic. It is pointed

out that the model given in [2]is incorrect. A correct model is derived in the present paper. The computer simulation shows that the model of Newcomb's circuit proposed in the present paper agrees with the experiment shown in [3].

MAA14-18 -- Time-Delay Neural Networks, Volterra Series, and Rates of Approximation

Sandberg, Irwin W., *The University of Texas at Austin*

We consider a large family of approximately-finite-memory casual time-invariant maps G from an input set S to a set of IR-valued functions, with the members of both sets of functions defined on the nonnegative integers, and we give an upper bound on the error in approximating a G using a two-stage structure consisting of a tapped delay line followed by a static neural network. As an application, information is given concerning the long-standing problem of determining the order of a Volterra-series approximation so that a given quality of approximation can be achieved. We have also obtained a corresponding result for the approximation of not-necessarily-casual input-output maps with inputs and outputs that may depend on more than one variable. These results are of interest, for example, in connection with image processing.

MAA14-19 -- Topological Dimensionality Determination and Dimensionality Reduction Based on Minimum Spanning Trees

de Figueiredo, Rui J.P. and Oten, Resnzi, *University of California, Irvine*

In the design of multidimensional systems for the analysis of complex data, an intelligent reduction of the data dimensionality is needed to enable its efficient and accurate processing without much loss of information. The underlying data transformation process can be implemented by nonlinearly mapping the high-dimensional data space onto a low-dimensional feature space where the mapping preserves the topological structure of the transformed data in the feature space as much as possible. This method is often referred to as Multidimensional Scaling (MDS). This paper describes a new MDS approach for feature extraction purposes. It consists of a fast hierarchical Minimal-Spanning-Tree-based method which minimizes the Sammon's criteria with a genetic algorithm. Results presented show that this new approach is promising for several applications.

MAA14-20 -- Investigations of Periodic Orbits in Electronic Circuits with Interval Newton Method

Galias, Zbigniew, *University of Mining and Metal*

We study the possibility of using interval Newton method for proving the existence of periodic orbits for models of electronic circuits. The advantages and limitations of the method are discussed. As an example a simple third order electronic circuit is considered, for which the existence of low-period unstable periodic orbits is proved.

MAA14-21 -- Stability Analysis and Robust Stabilization of a Class of Nonlinear Systems Based on Stability Radii

Jannesari, S., *Wichita State University*

The concept of Stability Radii, first proposed by Charles Van Loan [1], is a measure of robust stability for linear systems. In this paper, the exponential stability and robust stabilization of a class of nonlinear systems will be discussed. The class of nonlinear systems under consideration are the ones that can be separated into a nominal linear part plus a nonlinear perturbation with the linear part in Metzlerian form. It has been shown that if the norm of the nonlinear perturbations is bounded by the complex stability radius of the nominal system, then the entire system is stable. Here, we will apply an output feedback gain to the linear part of the system to increase its stability radius to be equal or greater than a given desired value.

MAA14-22 -- The Design and Fabrication of a Reconfigurable Hardware Testbed for the Interaction Analysis of Power Converters in a Reduced-Scale Navy DC Distribution System

Ashton, R.W.; and Ciezki, John G., *Naval Postgraduate School*

The authors present a reconfigurable dc distribution testbed that contains a number of converters, inverters and ajustable link impedances. The purpose of the hardware testbed is to study the interaction between nonlinear high-bandwidth converters in order to establish a means to develop theoretical stability criteria.

MAA14-23 -- A Computer Program for Accurate Time-Domain Analysis of 1D-Arrays of Chua's Oscillators

Bicy, Mario; Gill, Marco; Maio, Ivano; and Premoli, Amedeo, *Politecnico di Torino*

This paper describes a computer program for the time-domain analysis of one-dimensional arrays of Chua's oscillators.The implemented algorithm exploits the local connectivity, typical of cellular nonlinear networks, and the piecewise linear behavior of the v-i characteristic of the nonlinear elements to obtain an analytical expression of the solution. Examples demonstrate the accuracy and the efficiency, in terms of cpu-time, of the proposed approach with respect to standard simulation tools as SPICE.

MAA14-24 -- The Analysis of Tradeoffs between Power Section Hardware and Feedback Gains for a DC Distribution System DC-to-DC Converter

Ashton, R.W.; and Ciezki, John G., *Naval Postgraduate School*

The authors present a robust algorithm for controlling buck choppers that includes feedforward and droop. Averaged and detailed simulation models are used to optimize the design of the buck output capacitance and the feedback gains. In particular, an effect was made to simultaneously minimize voltage ripple and control efort while avoiding sustained oscillations 9kW chopper supplying a wide variety of loads including constant power loads.

MAA15 – Analog Filters — Poster Session

Chair: Phillip E. Allen

Georgia Institute of Technology

9:00 am – 12:30pm - ***Room: Serra Ballroom Back III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MAA15-1 -- Distortion Analysis of Switched-Current Circuits

Moschytz, George S. and Helfenstein, Markus, *Swiss Federal Institute of Technology*

A distortion analysis based on the large signal behavior of the basic switched-current memory cell is presented. In the first part, based on a closed form solution of the step response, distortion due to the settling error is addressed. In the second part, distortion caused by clock-feedthrough is analysed. The solutions are compared with simulated and/or measured results. Furthermore, harmonic terms above the fifth are shown to be negligible.

MAA15-2 -- Distortion Analysis of MOSFETs for Application in MOSFET-C Circuits

Schneider, Márcio Cherem, and Galup-Montoro, Carlos, *Universidade Federal de Santa Catarina*

The aim of this paper is to provide some guidelines on the design of MOS V-I converters. An explicit formula for the harmonic distortion based on an analytic model of the MOSFET has been derived for any inversion level. Experimental results for the distortion in the MOSFET V-I characteristics as well as biasing and tuning strategies applied to MOSFET-C filters are presented.

MAA15-3 -- Design and Implementation of an Algorithmic S2I Switched-Current Multiplier

Pineda de Gyvez, Jose, *Texas A&M University;* and Manganaro, Gabriele,*Texas Instruments, Inc.*

The analysis, design and implementation of a S2I switched-current multiplier is presented. A thorough circuit analysis of the multiplier's and its non-idealities is presented both with a design procedure. It has been implemented using a 2mm n-well CMOS technology. The following are brief highlights of the measurement results: i) 0.425 millions of multiplication per second ii) 1.7% total harmonic distortion for a sinusoidal of 35mA (50Hz) iii) 206KHz of bandwidth iv) 50dB of SNR and v) 0.3mW zero input power consumption for a +/-3V power supply. A complete set of detailed experimental results is provided in the paper.

MAA15-4 -- Simulation of Coupled Tuned Circuits Using CFOAs

Aronhime, Peter, and Deng, Jie, *University of Louisville*, and Maundy, Brent, *University of Calgary*

An active RC voltage-mode circuit that mimics the behavior at low frequency of a bandwidth-tunable bandpass filter as realized by a double-tuned circuit is converted to a current-mode circuit using commercially available current-feedback op-amps. Analyses and simulations show that the new current-mode circuit can operate relatively accurately in the neighborhood of 300 kHz using passive elements determined by ideal analysis.

MAA15-5 -- Improved Fully Differential Circuits Using Hybrid Structures

Walker, Paul D., *Silicon Systems*, and Green, Michael M., *University of California, Irvine*

Fully differential circuits offer improved dynamic range over their single-ended counterparts, however such circuits require additional common-mode feedback. A method for implementing fully differential circuits without common-mode feedback was presented previously by the authors, however circuits designed using this approach lack common-mode signal rejection. In this paper we examine a hybrid fully differential circuit, which combines both conventional fully differential circuits with common-mode feedback and blocks without common-mode feedback in order to utilize the advantages of both approaches.

MAA15-6 -- Feasible Designs for High Order Switched-Current Filters

Sewell, John Isaac, and Ng, Andrew, *University of Glasgow*, Lo,Chun-Keung, Lo, Chun-Keung, and Lo, Chun-Keung, *The Hong Kong University of Science and Technology*, and Li, Dongju, *Tokyo Institute of Technology*

Fully-balanced integrators based on S2I type memory cells are introduced for realising bilinear-LDI switched-current ladder filters. The problems of high component spreads and large silicon area encountered in very high order designs are overcome by adopting modified approximation and prototype ladder manipulation techniques, resulting in a typical example of a 21st order elliptic lowpass filter with a spread of 13.63. Modifications that allow for simplified input stages are also presented.

MAA15-7 -- Accurate CMOS Switched-Current Divider Circuits

Wey, Chin-Long, *Michgan State University*, and Wang, Jin-Sheng, *Michigan State University*

This paper presents a highly accurate current divider using switched-current (SI) technique. The circuit accurately divides an input.current by two with 3 cycles at each iteration. The accuracy of the division increases as the number of iterations increases. In practice, however, the accuracy is limited due to the clock-feedthrough errors. The issue of accuracy limitation is addressed. The extension to array structures for low-power/low-voltage A/D and D/A converter circuit designs is also discussed.

MAA15-8 -- Fundamental Frequency Limitations in Current-Mode Sallen-Key Filters

Moschytz, George S. and Schmid, Hanspeter, *Swiss Federal Institute of Technology*

Single-amplifier filter biquads and especially Sallen-Key filters are widely used to build higher-order filter cascades. This paper investigates high-frequency current amplifier non-idealities and their effects on all-pole Sallen-Key filter biquads. It is shown that a non-ideal current amplifier input causes parasitic zeros in the filter transfer function, and thus imposes fundamental limitations on the reliable pole frequency. Design equations are given, providing compensation for the amplifier's port impedances and its phase lag, by predistortion of the component values. It is also shown how design specifications for a current-amplifier can be derived from the filter specification, minimizing the amplifier's power dissipation. Finally, a video-frequency lowpass filter is discussed.

MAA15-9 -- BiCMOS OTA for High Q Very High Frequency Continuous-Time Bandpass Filters

Minot, Sophie, and Degrugillier, Dominique, *Enst de Bretagne*

In this paper, we show that BiCMOS technology is really suited to the implementation of high-Q, VHF, Gm-C continuous-time bandpass filters. The major problem of such filters is the output resistance value of the transconductors which must be very high. The design approach is based on the use of a negative resistance element in BiCMOS technology which allows the output resistance value to be increased close to 50 MW without any limitation in the bandwidth of the transconductor circuit. Simulation results of a biquadratic bandpass filter with center frequency fo=84.6MHz and quality factor Qo=30 conclude the paper.

MAA15-10 -- Automatic Tuning of Frequency and Q-Factor of Bandpass Filters Based on Envelope Detection

Karsilayan, Aydin Ilker, *Portland State University*

The paper discusses an approach using very simple tuning circuitry based on the envelope detection method. A second-order band-pass filter is used as a demonstration vehicle. The complete tuning circuit consists of frequency and Q-factor tuning blocks, and operates on a 3V power supply. Due to its simplicity, this method can be used for automatic tuning of high-Q bandpass filters at very high frequencies with very little circuit overhead.

MAA15-11 -- A CMOS Multiplier/Divider Based on Current Conveyors

Cattet, Stephane, *CPE Lyon*

The design of a CMOS current conveyors based analog multiplier/divider is presented. A transresistance amplifier using four current conveyors has been designed in order to achieve a 80MHz bandwidth in a standard 0.8 um CMOS process. Two four MOSFETs transconductors perform the multiplication and the division. Because of the low area dedicated to the current conveyor, the proposed circuit is really area-efficient for high integration.

MAA15-12 -- Reducing Spread Resistance in High Q State Variable Filters

Báez-López, David J.M., Guillermo, Espinosa F. V., and Silva-Martinez, Jose, *Instituto Nacional de Astrofísica, Optica y Electrónica*

In this paper we propose a method to reduce the resistance spread in the high Q realizations of the KHN and Tow-Thomas state variable filters. This resistance spread is reduced by noting that a single resistor controls the value of the pole Q, thus by substituting this resistor by a T of resistor it is possible to reduce the spread by up to a factor of 10. Simulations confirm the proposed technique.

MAA15-13 -- Low-Voltage S2I and S3I Cells for Sigma-Delta Signal Processing

Musil, Vladislav, and Simek, Petr, *Technical University of Brno*

The paper presents novel implementations of switched-current cells suitable to operate with 1.5V supply voltage. The cells based on S2I and S3I principles are evaluated for the low-voltage operation and maximum achievable dynamic range. A second order sigma-delta modulator is simulated using a low voltage cell. Simulated output spectrum analyses are presented.

MAA15-14 -- Two-Step Current-Memory Cells with Optimal Dynamic Range for Advanced CMOS Technologies

Kaiser,Andreas, *IEMN-ISEN*

Improved two-step current-memory cell architectures employing current conveyors are proposed and compared with conventional ones over a wide range of technologies. Special emphasis is given to the evaluation of performance on very advanced state-of-the-art CMOS technologies and the

operation at low supply voltages. Up to 50% power savings can be expected with respect to conventional cells of same performance.

MAA15-15 -- A 4-Transistor Euclidean Distance Cell for Analog Classifiers

Cilingiroglu, Ugur, Aksin, and Devrim Yilmaz, *Istanbul Technical University & ETA ASIC Design Center*

The area efficiency of a high throughput parallel classifier depends strongly on the area of the basic distance cell because classifier architectures contain a large array of such cells. For this reason, reducing the circuit complexity of a distance cell is expected to have a magnified impact on the overall size. A new squared Euclidean distance cell configuration comprising four MOSFETs and two capacitors is proposed. The cell is based on symmetrical capacitive template storage and current domain readout, which help reduce size while increasing speed and precision. A typical cell design in a mainstream 0.8 micro meter CMOS technology occupies 17.2 times 21.9 square micro meter. Silicon area representing an area density of 2650 cells per square millimeter. The article includes a description and analysis of the circuit, identifies design constraints and presents an error analysis.

MAA15-16 -- Multiple-Input Translinear Element Networks

Minch, Bradley A., and Hasler, Paul, *Georgia Institute of Technology*, and Diorio, Chris.*University of Washington*

We describe a class of nonlinear circuits that accurately embody product-of-power-law relationships in the current signal domain. We call these circuits multiple-input translinear element (MITE) networks. A MITE is a circuit element that produces an output current that is exponenial in a weighted sum of its input voltages. We describe intuitively the basic operation of MITE networks and we show experimental data from a squaring-reciprocal circuit breadboarded from bipolar-floating-gate MOS (biFGMOS) MITEs that we fabricated in a 2-um double-poly CMOS process available through MOSIS.

MAA15-17 -- UCM - Universal Current-Mode Structures

Galvez-Durand, Federico, *Universidade Federal do Rio de Janeiro*

A novel current-mode analogue continuous-time filter synthesis technique is proposed based on a transformed set of state-equations, that allow the utilization of only current-mode linear lossy-integrators implemented using standard current mirrors; also a novel current-mode gyrator is introduced. The technique has been successfully used for synthesizing low-voltage 5th order lowpass, highpass, bandpass and stopband Chebyshev filters from passive doubly loaded ladder prototypes. SPECTRE simulations using CMOS standard process BSIM3 parameters have shown these filters perform well, exhibiting a THD less than 1% at 100 kHz for a 40 mV output (1 uA input current) while the bias current per transistor is 10 uA. Also, a Monte Carlo analysis has shown these filters preserve the low sensitivity inherent to the passive ladder prototype. The reduced number of small transistors necessary leads to small integration areas. The circuits have been fed with +- 1.5 V power supplies.

MAA15-18 -- Generation of Canonic Multiple Current Output OTA Sinusoidal Oscillators with Non-Interacting Controls

Tao, Yufei, and Fidler, J. Kel, *University of York*

In this paper a method of systematically generating sinusoidal oscillators with non-interactiing controls using multiple current output Operational Transconductance Amplifiers (MO-OTAs) is introduced. This is an exhaustive method through which all the desired circuits belonging to the investigated class can be generated. The frequency of oscillation (FO) and condition of oscillation (CO) of the oscillators derived using this method is realized electronically with the two transconductance parameters of the MO-OTA. Five novel canonic oscillators with both capacitors grounded are obtained, which can also realize second order bandpass (BP) transfer functions without changing the topologies.

The natural frequency and the bandwidth of three of the BP filters can be tuned independently by the two transconductance parameters.

MAA15-19 -- Very Low-Distortion Fully Differential Switched-Current Memory Cell
Martins, Jorge Manuel, *INESC/IST*

This paper proposes a very low distortion fully differential Switched-Current memory cell, based on the opening of the memory switch at a constant voltage. We show that in two previously proposed single-ended cells [1,2] this principle does not lead to low harmonic distortion, because the distortion is also a function of the signal-independent clock feedthrough. SPICE simulations indicate that the proposed cell achieves a level of distortion of about -100 dB, which is more than two orders of magnitude below the level achieved with basic SI cells. The performance of the proposed cell approaches that of state-of-the-art Switched-Capacitor circuits.

MAA15-20 -- Reliable Analog Bandpass Signal Generation
Veillette, Benoit R., and Roberts, Gordon W., *McGill University*

A novel method for generating bandpass type signals is introduced. A phase function is turned into a jittery bandpass signal using a delta-sigma modulator and digital phase modulation. This signal can be used to verify the correct operation of a charge-pump phase-locked loop. After validation of this circuit, more complex communication signals such as GMSK may be generated for test purposes. As all components are digital or may be tested digitally, this scheme is amenable to built-in self-test.

MAA15-21 -- Noise Analysis of Switched-Current Circuits
Jorgensen, Ivan H.H., *Technical University of Denmark*, and Bogason, Gudmundur, *OTICON A/S*

The understanding of noise in analog sampled data systems is vital for the design of high resolution circuitry. In this paper a general description of sampled and held noise is presented. The noise calculations are verified by measurements on an analog delay line implemented using switched-current (SI) technique.

MAA15-22 -- Phase-Tunable CMOS Triode Transconductor
Jun, Sibum, *LG Semicon Co., Ltd.* and Ahn, Su Jin, *POSTECH*

An alternative implementation of the fully differential CMOS triode transconductor, in which adopts a fully differential amplifier, has been described. The resulting circuit is totally fully differential and provides two independent control terminals applicable to frequency-tuning and Q-tunings.

MAA15-23 -- Efficient Design of Switched-Current Lowpass Elliptic Wave Filters Using Bruton Transformation
Lancaster, Jason David, Al-Hashimi, Bashir, and Moniri, Mansour,*Staffordshire University*

This paper describes how the Bruton transformation facilitates the development of an efficient design methodology for switched-current elliptic lowpass wave filters. Wave models for the design methodology including frequency dependent negative resistance (FDNR) component, capacitive source and capacitive load are presented.The proposed design technique offers a significant reduction in the filter transistor count. For example, a 7th order lowpass elliptic filter utilises 20% less delay elements and 16% less current mirrors when compared with a recently reported design technique. This is achieved by having a filter structure with a large number of resistors and simplified series adapters. Simulated results based on a typical CMOS process for a lowpass elliptic filter with a cutoff frequency of 100 KHz and a sampling frequency of 1 MHz are included.

MAA15-24 -- Ladder Decompositions for Wideband Switched-Current Filter Applications

Sewell, John Isaac, and NG,Andrew *University of Glasgow*

Methods for designing switched-current ladder filters for wideband applications are presented. By performing UL-LU and LU-UL decompositions on the z-domain matrix description of a bilinear-transformed passive ladder, filter structures are derived which preserve low passband sensitivity even for large relative bandwidths. Derivation procedures are outlined and illustrated by the example of a 10th order LU-UL bandpass filter. The switched-current filters are realised using Euler-type integrators based on S3I cells. A comparison of the properties of different structures demonstrate the advantages of the UL-LU and LU-UL methods.

MONDAY AFTERNOON -- JUNE 1, 1998

MPA1 – Multidimensional Signal Processing

Chair: M. Omair Ahmad

Concord University

2:00 pm – 5:30pm - ***Room: Colton I***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA1-1 -- Symmetry in the Frequency Response of Two-Dimensional {gamma1, gamma2} Complex Plane Discrete-Time Systems

Reddy, Hari C., *California State University, Long Beach,* Khoo, I-Hung, *University of California, Irvine;*Rajan. P. K.; *Tennessee Tech University, and* Stubberud, Allen R., *University of California, Irvine*

This paper presents the constraints on two-dimensional gamma-domain polynomials so that they possess various types of symmetries in their magnitude functions. {gamma1,gamma2} complex bi-plane is shown in Figure 3. Refering to the parameter (delta) in the figure, it is concluded that new symmetry conditions derived in gamma-plane converge to those of 2-D continuous-time systems as delta tends to zero. For analog sampled-data systems, delta can be treated as a sampling period, otherwise it is simply treated as a design parameter.

MPA1-2 -- FPGA Implementation of Hierarchical Clustering Algorithms

Niamat, Y., Bitter, D., and Jamali, M.M., *The Universityof Toledo*

In this paper, the design and implementation for computing the Single Linkage(SLINK) and Complete Linkage(CLINK) clustering algorithms on a Field Programmable Gate Array (FPGA) are presented. This research seeks to extend the authors' previous work in which novel systolic arrays for implementing the SLINK hierarchical clustering algorithm were presented. As is well known, hierarchical clustering algorithms find applications in many engineering areas, including pattern classification and image processing. However, the execution of these algorithms require considerable CPU time which makes them unsuitable for real-time applications. Our motivation for performing this research is to reduce the CPU time taken for executing the algorithms under discussion. In the present work, our focus is on the implementation of the proposed systolic arrays on a reconfigurable architecture, namely, a Xilinx FPGA. The reconfigurability aspect of the FPGA permits the implementation of both the SLINK and CLINK algorithms on the same FPGA.

MPA1-3 -- Multidimensional Digital Filter Approach for Numerical Solution of a Class of PDEs of the Propagating Wave Type

Basu, Sankar, *IBM T. J. Watson Research Center*; and Zerzghi, Amanuel, *Lucent Technologies*

Numerical schemes exploiting passive multidimensional digital filtering methods for the solution of partial differential equations describing a large variety of physical systems are studied. We consider a system of linear differential equations in (n+1) variables that model a variety of physical phenomena. The technique involves mapping the PDEs into a (n+1) dimensional passive digital filter essentially via a rotation of the space-time coordinates. The passive digital filter is then synthesized by means of internally or structurally passive building blocks. Similar solutions have been proposed in the very recent past using wave digital filter principles. While this technique relies heavily on the formalism of classical analog network theory, our method is more akin to the so called orthogonal filter principle, and is believed to be more direct without having to explicitly use any result from the synthesis theory of classical networks.

MPA1-4 -- On (p,q)-Markov Covers for 2-D Separable Denominator Systems

Sreeram, V. and Liu, W.Q., *University of Western Australia*; Agathoklis, Pan, *University of Victoria*

In this paper, a technique for obtaining (p,q)-Markov Cover models for 2-D separable denominator systems is presented. This is an extension of the work on q-Markov Cover model reduction technique for 1-D systems and is based on 2-D impulse response Gramians.

MPA1-5 -- Weighted L2 Sensitivity Minimization of 2-D Discrete Systems

Hinamoto, Takao and Yokoyama, Shuichi, *Hiroshima University*; Lu, Wu-Sheng, *University of Victoria*

In this paper, the problem of synthesizing the finite-word-length2-D state-space filter structures with minimum weighted L2 sensitivity is considered. First, a frequency-weighted sensitivity measure is defined in place of a usual sensitivity measure. This is based on a pure L2-norm. Next, an iterative procedure is developed for obtaining the optimal coordinate transformation that minimizes the weighted L2 sensitivity measure. Applying the proposed procedure, the estimate at each iteration can be calculated analytically. Finally, a numerical example is given to illustrate the utility of the proposed technique.

MPA1-6 -- The Two Dimensional Lapped Hadamard Transform

Muramatsu, Shogo, Yamada, Akihiko, and Kiya, Hitoshi, *Tokyo Metropolitan University*

In this paper, a 2-D binary-valued (BV) lapped transform (LT) is proposed. The proposed LT has basis images which take only BV elements and satisfies the axial-symmetric (AS) property. In 1D, there is no 2-point LT with the symmetric basis vectors. Hence, in 2D, there is no 2 x 2-point separable ASLT. By taking non-separable BV basis images, this paper shows that a 2 x 2-point ASLT can be obtained. For its similarity to the Hadamard transform (HT), this paper refer to it as the lapped Hadamard transform (LHT). The effcient implementation is also given.

MPA1-7 -- A New 2-D Adaptive Filter Using Affine Projection Algorithm

Muneyasu, Mitsuji, and Hinamoto,Takao, *Hiroshima Univeristy*

This paper proposes a realization of two-dimensional (2-D) adaptive finite impulse response (FIR) filters using affine projection method. The convergence property of the proposed algorithm is superior to that of the 2-D least mean square (LMS) and normalized LMS (NLMS) algorithms. This algorithm has properties that lie between those of NLMS and recursive least squares (RLS) algorithms. The generalization of the proposed algorithm is also discussed. To illustrate the utility of the proposed technique, this filter is applied to the 2-D system identification.

MPA1-8 -- A Stability Test of Reduced Complexity for 2-D Digital System Polynomials

Bistritz, Yuval, *Tel Aviv University*

A new algebraic test for deciding whether a 2-D (bi-variate) polynomial has all its zeros in the interior of the unit bi-circle is presented. The testing of a polynomial of degree (n1,n2) is performed by n1 n2 + 2 unit circle tests of 1-D polynomials of degree n1 or n2 plus one of degree 2 n1 n2 and it can be carried out in a very low (apparently unprecedented) count of approximately 1.5 n1 n2 ^3 + 2 n1 ^2 n2 ^2 real flops.

MPA2 Optimization of Subband Coders Based on the Input
Special Session

Chair: P.P. Vaidyanathan
California Institute of Technology

2:00 pm – 5:30pm - ***Room: Colton II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA2-1 -- Enhancing the Performance of Subband Audio Coders for Speech Signals

Malvar, Henrique S., *Microsoft Research*

Transform or subband audio coders can deliver high quality reconstruction at rates around two bits per sample. Most quantization strategies take into account masking properties of the human ear to make the quantization noise less noticeable. In this paper we describe a new coder in which we extend such quantization strategies by incorporating run-length and arithmetic encoders. They lead to improved performance for quasi-periodic signals, including speech. The quantization tables are computed from only a few parameters, allowing for a high degree of adaptability without increasing quantization table storage. To improve the performance for transient signals, the coder uses a nonuniform modulated lapped biorthogonal transform with variable resolution without input window switching. Experimental results show that the coder can be used for good quality signal reproduction at rates close to one bit per sample, and quasi-transparent reproduction at two bits per sample.

MPA2-2 -- Optimized Orthogonal and Biorthogonal Wavelets Using Linear Parameterization of Halfband Filters

Lu, Wu-Sheng, and Antoniou, Andreas, *University of Victoria*

A new method for the construction of compactly supported orthogonal and biorthogonal wavelets that can be optimized for specific applications is proposed. Unlike existing methods for the parameterization of orthogonal wavelets, the new method is based on a linear parameterization of all halfband filters. The linear dependence of the halfband filters on a "free" parameter vector considerably facilitates the subsequent numerical optimization through which optimized wavelets are constructed. Biorthogonal wavelets are obtained by factorization of a polynomial representing the parameterized halfband filkters while orthogonal wavelets are constructed by imposing nonnegativity on the parameterized halfband filters followed by spectral factorization. The well-known Daubechies orthogonal wavelets and the Cohen-Daubechies-Feauveau biorthogonal wavelets can be viewed as subsets in the parameterized orthogonal and biorthogonal wavelet classes, respectively. Applications of this parameterization-based optimization of wavelets to signal coding are discussed.

MPA2-3 -- Optimization of High-energy-compaction, Nearly-orthonormal, Linear-phase Filter Banks

Yang, Xuguang; Ramchandran, Kannan; and Moulin, Pierre, *University of Illinois at Urbana-Champaign*

In this paper, we design two-channel, perfect-reconstruction, linear-phase, biorthogonal filter banks that maximize orthonormality subject to structural constraints on the filter bank. These structural constraints may be adjusted so as to provide various degrees of energy compaction. The applications targeted are in compression. Proper cost functions are formulated and an efficient signal-adaptive optimization algorithm is proposed. Our algorithm is motivated by a number of interesting properties of the correlation matrix of typical signals and images, and efficiently uses the degrees of freedom in the parameterization of perfect reconstruction filter banks. The algorithm provides different levels of tradeoff between the energy compaction and approximate orthonormality goals. Comparisons with the popular Daubechies 9-7 filter bank show significant improvements in terms of orthogonality and energy compaction.

MPA2-4 -- Post-processing of Compressed Images with Side Information

Nosratinia, Aria, *Rice University*

This paper investigates the usage of side information for linear post-processing in subband image compression systems. In particular, side information is used to determine a custom synthesis filter bank for each image. It has been known that prefect reconstruction filters are not optimal in the presence of quantization noise. However, most of the previous related work concentrated on optimizing analysis-synthesis pairs jointly, which requires very strong conditions. Limiting our attention to the decoder, we find optimal synthesis filters by solving a system of regression equations. Neither high-rate quantization, whiteness of the quantization noise, nor optimality of the quantizer is assumed. By allowing transmission of side information, we take a deterministic approach, thus finding the best reconstruction without any constraints such as stationarity. Optimal coefficients are independent of the internal machinery of the quantizers, and can therefore be used with ``canned'' software packages for post-processing purposes.

MPA2-5 -- A Survey of the State-of-the Art and Utilization of Embedded, Tree-Based Coding

Pearlman, William A., *Rensselaer Polytechnic Institute*; and Said, Amir, *Iterated Systems, Inc*.

We review first the development of tree-based, embedded image coding. We then explore their use with different image transformations, the reasons for their effectiveness and low complexity, their flexibility and incorporation into state-of-the-art compression systems.

MPA2-6 -- A Performance Study of DCT and Subband Codecs with Zero-Zone Quantizers

Ramkumar, Mahalingam and Akansu, Ali N., *New Jersey Institute of Technology*

It has been shown in [1,2] that zero-zone quantizers offer very good R-D tradeoffs, especially at low bit-rates, in spite of their simplicity in implementation and concept. In [1] the performance of such codecs for still and moving images were reported for a dyadic 10-band subband coder. In this paper we extend those results to other subband image codecs, and DCT, and compare their performances

MPA2-7 -- The Role of the Discrete-Time Kalman-Yakubovitch-Popov Lemma in Designing Statistically Optimum Fir Orthonormal Filter Banks

Tuqan, Jamal, and Vaidyanathan, P.P., *California Institute of Technology*

We introduce a new approach to design FIR energy compaction filters of arbitrary order N. The optimization of such filters is important due to their close connection to the design of an M-channel orthonormal filter bank adapted to the input signal statistics. The novel procedure finds the optimum product filter Fopt(z) = Hopt(z)Hopt(z-1) corresponding to the compaction filter Hopt(z). The idea is to express F(z) as D(z)+D(z-1) and reformulate the compaction problem in terms of the state space realization of the sausal function D(z) is guaranteed to be a global optimum due to the convexity of the new formulation . The new design method can be solved quite efficiently and with great accuracy using recently developed interior point methods and is extremely general in the sense that it works for any chosen M and any arbitrary filter length N. Finally, obtaining Hopt(z) from Fopt(z) does not require an additional spectral factorization step. The minimum phase spectral factor can be obtained automatically by relating the state space realization of Dopt(z) to that of Hopt(z).

MPA2-8 -- Design of Linear Phase Paraunitary Filter Banks with Suboptimal Coding Gain without Nonlinear Optimization

Ikehara, Masaaki, *Keio University and* Nguyen, Truong Q., *Boston University*

This paper presents a design method for linear phase paraunitary filter banks (LPPUFB) with suboptimal coding gain without nonlinear optimization. First, we design a lowpass filter with some regularities and then M/2-1 highpass and bandpass filters are designed such that each filter has minimum compaction gain. The cost function which consists of the frequency constraint, orthogonal condition and the variance of output signal is expressed in quadratic form of the filter coefficients. Consequently, the cost function can be minimized by solving linear equations iteratively without using nonlinear optimization.

MPA 3 Memory, Adaptation and Learning Special Session

Chair: Gert Cauwenberghs

John Hopkins University

Organizers: Gert Cauwenberghs

John Hopkins University
Fathi Salam
Michigan State University
Paul Hasler
Georgia Institute of Technology

Sponsor: IEEE CAS Society Technical Committee on Neural Systems and Applications

2:00 pm – 5:30pm - ***Room: Colton II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA3-1 -- A Four-Quadrant Floating-Gate Synapse

Hasler, Paul,;*Georgia Institute of Technology*, Diorio, Chris;*University of Washington* and Minch, Bradley A., *Cornell University*

We present experimental measurements from a floating-gate synapse that simultaniously computes four-quadrant products of its input and weight values, and computes a four-quadrant correlation, typical of hebbian and backpropagation learning rules, between the input and drain voltages. Our four-quadrant synapse is built from two source-degenerated pFET synapses. We build this new type of floating-gate synapse by adding weak exponential feedback to the source of a floating-gate pFET synapse. This floating-gate synapse has the unique dynamical properties that the oxide currents provide stabilizing feedback to the floating gate and to the drain. This four-quadrant synapse can become the fundamental building block of many continuous-time neural-network learning algorithms.

MPA3-2 -- Programmable Current Mode Hebbian Learning Neural Network using Metallization Programmable Cells

Swaroop, B.;Kozidu, M.N and Akers, Lex A, *University of Texas at San Antonio*

The design and performance of a Hebbian learning based neural network is presented in this work. In situ analog learning was employed, thus computing the synaptic weight changes continuously during the normal operation of the artificial neural network (ANN). The complexity of a synapse is minimized by using a novel device called the Programmable Metallization Cell (PMC) [1].Simulations with circuits with three PMCs per synapse showed that appropriate learning behaviour was obtained at the synaptic level.

MPA3-4 – Design of a Programmable Pulse-Coded Neural Processor for Hippocampal Region

Tsai, Richard H.; Sheu, Bing J.; and Berger, Theodore W., *University of Southern California*

Rapid advances in submicron microelectronic technologies have made possible the integration of millions of transistors on a sigle silicon chip for complex signal processing and control functions. The hippocampal region of the brain system can be analyzed with a nonlinearsystem modeling approach. The input-output relationship of the neural units is represented by the kernel functions of various complexities. The modeling expressions of the first and second order kernels are computed in analog current-mode instead of digital format in order to fully explore massively parallel processing capability of the neural networks. A programmable pulse-coded neural network based on the hippocampal kernel functions can process the pulse information efficiently. The model-based approach saves silicon area and achieves adequate accuracy level. Circuit-level simulation results and experimental data are also presented

MPA3-5 -- A Robust Hybrid Neural Architecture for An Industrial Sensor Application

Djahanshahi, Hormoz; MacLean B. Ahmadi, Majid, Jullien, Graham A., and Miller, William C., *University of Windsor*

A programmable hybrid neural network architecture has been used to implement a smart optical sensor with focal-plane pattern classification for a flexible manufacturing cell environment. The network contains an integrated photosensitive array based on modified photo BJTs as input to a fully-connected MLFF neural classifier. The architecture features a distributed neuron realization that employs a number of active nonlinear resistor circuits operating in parallel. It minimizes the effect of parameter variations due to non-uniform device fabrication over the die surface. Moreover, due to the modularity of the architecture and locality of interconnections, synaptic density has been doubled in comparison with a conventional realization. A photosensor-classifier chip consisting of a 2-D array of 64 neural-based smart pixels and additional neural network circuits has been fabricated. The proposed architecture has been implemented in both CMOS and BiCMOS process technologies as part of a sensor optimization study.

MPA3-6 -- Design of an Analog CMOS Self-Learning Multilayer Perceptron Chip

Bo, G.M.; Caviglia, D.D., Chibli, H., and Valle, M, *University of Genoa*

In this paper we present the analog CMOS design of a Multi-Layer Perceptron network with on-chip by-pattern Back-Propagation learning. The learning algorithm is based on a local learning rate adaptation technique which makes the on-chip implementation more efficient in terms of convergence speed. Circuit simulation results validate the network behavior.

MPA3-7 – Hardware Compatible Learning for Neuro-Fuzzy Controllers

Vidal-Verdú, Fernando; Navas-Gonzalez, Rafael; and Rodriquez-Vasquez, Angel, *University of Málaga.*

Learning algorithms have become of great interest to be applied not only to neural or hybrid neuro-fuzzy systems, but also as a tool to achieve a fine tuning of analog circuits, whose main drawback is their lack of precision. This paper presents accurate, discrete-time CMOS building blocks to implement learning rules on-chip. Specifically, a voltage mode high precision comparator as well as an absolute value circuit. These blocks, plus multiplexing in time techniques, are used to build a circuit to determine the polarity of the learning increments. An exemplary circuit has been simulated with HSPICE with the parameters of a 1um CMOS technology. Statistical variations of

technological parameters were considered.The results show that all curves from 30 runs of a montecarlo analysis behave as expected, and at least 8 bits of resolution are achieved by the proposed techniques.

MPA3-8 – On-Line Modeling and Control Using a CMOS Analog Temporal Neuroprocessor

Salam, Fathi M., *Michigan State University*

We present results of several experiments of a neural network with temporal learning on a single chip. The single chip configuration is a 2-d scalable array with learning constructed via simple modular CMOS building blocks. We report on learning prototype periodic temporal signals, which may be displayed as a closed curve, a figure-8 shape, or an arbitrary periodic or aperiodic shapes in the state space. The experiments demonstrate the instantaneous learning by the chip of these shapes.

MPA3-9 -- A Micropower Learning Vector Quantizer for Parallel Analog-to-Digital Data Compression

Lubkin, Jeremy and Cauwenberghs, Gert, *Johns Hopkins University*

An analog VLSI architecture for learning vector quantization (LVQ), with on-chip adaptation and dynamic storage of the analog templates, ispresented. The architecture extends to Fuzzy ART and Kohonen self-organizing maps through digital programming. The analog memory and adaptive element of the LVQ cell comprise 6 MOS transistors and one capacitor, and provide for robust self-refresh of the dynamic analog storage. Total cell size including distance and adaptive computations is 80 X 70 lambda in scalable MOSIS technology. Experimental results from a fabricated 16 X 16 cell prototype in 2 um CMOS are included.

MPA4 Multimedia Systems and Processing

Chair: Bing Sheu

University of Southern California

2:00 pm – 5:30pm - ***Room: Ferrante I***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA4-1 -- Bandwidth Planning in Near Video-on-Demand

Chan, Shueng-Han Gary; Tobagi, Fouad; and Ko, T.M., *Stanford University*

In near video-on-demand, requests for a video file arriving within a period of time are batched together and served with a single multicaststream; thereby reducing the bandwidth requirement compared with the unbatched case. Since the delayed users may renege (and hence causing revenue loss to the service providers), the design of a near video-on-demand system has to meet users' delay expectation. In this paper, we specify the minimum number of streams required for a video file so that only a small fraction of the users experience delay higher than a certain value. Trade-off issues between user's delay tolerance and the required number of streams are also addressed.

MPA4-2 -- A Low-Cost Architecture Design with Efficient Data Arrangement and Memory Configuration for MPEG-2 Audio Decoder

Tsai, Tsung-Han, Chen, Liang-Gee, Huang, Sheng-Chieh, and Chang, Hao-Chieh, *National Taiwan University*

The paper describes a low-cost MPEG-2 audio decoder with a modified fast algorithm for decoding. In the modified decoding scheme, the computation amount of the bottleneck module can be reduced into one-forths of the original one. Also, the major memory storage only requires half size of the standard synthesis subband filterbank. The decoder is developed for the approaches of simplicity and low-cost architecture design, with the techniques of intelligent data arrangement and memory configuration.

MPA4-3 -- Real-time Digital Video Stabilization for Multi-media Applications

Ratakonda, Krishna, *University of Illinois at Urbana-Champaign*

Amateur digital video footage, shot with a hand-held camera, is characterized by visually annoying, jerky movement between successive frames. In this paper a fast and robust image stabilization technique is presented to remove the effects of unwanted camera motion while not effecting true pans or zooms. Unlike other image stabilization techniques, which are typically used as a pre-processing step to more complicated image processing operations, the proposed technique is specifically aimed at providing ``visually jerk-free video'' for consumer viewing. Empirical evidence suggested that a simple global translational model for each pair of successive images followed by

local integration of cumulative motion is sufficient for this purpose. We use a novel technique to estimate the translational motion model, which reduces the total computational burden to less than computation/pixel, while providing robust jerk elimination, thus making real-time operation possible on most PC/UNIX platforms. Tests with a number of video sequences have shown the efficacy of the proposed method.

MPA4-4 -- Scalable Image Sensor/Processor Architecture with Frame Memory Buffer and 2-D Cellular Neural Network

Cho, Kwang-Bo; Sheu, Bing J.; and, Young, Wayne C. *University of Southern California*

The compact, high computing power systems become feasible with significant progress in the research and development of advanced computing architecture and array processing. Scalable image sensor array processor with frame memory buffer and cellular neural network (CNN) for nearest neighbor interaction has been developed in a 0.5um HP CMOS technology. The CNN with analog programmable weights was constructed with compact mixed-signal VLSI circuit components in the current-mode techniques. The low voltage, low power operation is supported with the current mode scheme which scales well with the supply voltage. VLSI design of a variable gain neuron circuit can be incorporated into the prototype to realize the optimal solution capability using hardware annealing.

MPA4-5 -- The BJT-Based Silicon-Retina Sensory System for Direction and Velocity-Selective Sensing

Jiang, Hsin-Chin and Wu, Chung-Yu,, *National Chiao Tung University*

In this paper, a BJT-based silicon-retina sensory system for direction- and velocity-selective sensing is proposed and implemented. This detector can selectively detect the specified direction and speed of moving object image in 2-dimension. The basic detection cell consists of one BJT-based silicon retina cell, one current-mode edge extractor, two delay paths, and four correlators. The signals which are used to be correlated are binary pulsed signals. The BJT-based silicon retina with the current-mode edge extractor can be easily incorporated into various motion measurement systems and associated image processing neural network to reduce the hardware complexity for VLSI implementations and provide robust edge detection. Using the proposed architecture, an experimental 2-D 32x32 motion measurement chip has been fabricated by using 0.6 um CMOS technology. The functions of the proposed sensory system are also verified through measurements.

MPA4-6 -- New View Generation from A Video Sequence

Chen, Szo Sheng and Hang, Hsueh-Ming, *National Chiao Tung University*

The problem of three-dimensional (3-D) scene representation and view generation is a new subject in video signal processing. Our goal is to construct a new scene at a different viewing position based on a sequence of captured images. The method proposed here does not make use of a solid 3-D model of physical objects. We decompose the image into layers based upon the motion maps derived from consecutive frames of an image sequence, and then synthesize a new view by recomposing the layers. In this process, accurate motion information estimation and consistent layer data aggregation are two critical steps. Some results using a real image sequence are shown at the end.

MPA4-7 -- Fast Approach For Detecting Human Faces In A Complex Background

Lam, Kenneth, *The Hong Kong Polytechnic University*

Human face detection is an important capability with a wide range of applications, such as human face recognition, surveillance systems, human-computer interfacing, video-conferencing, etc. In most such applications, the existence of human faces and their corresponding locations must be found. In other words, a reliable and fast method for detecting and locating face regions is of practical importance. In this paper, possible face region candidates in an image with a complex background are identified by means of the valley features on the eyes. These valley features are considered to belong to the eyes of a human face if they satisfy the local properties of the eyes. A pair of these features is amtched if their Gabor features are similar; a face region is then formed. Each of the face region candidates is then further verified by matching it to a human template, and by measuring its symmetry. Experiments show that this approach is fast and reliable.

MPA4-8 -- Memory Based Architecture for Real-time Convolution with Variable Kernels

Moshnyaga, Vasily, *Fukuoka University*, Suzuki, Kazuhiro and Tamaru, Keikichi, *Kyoto University*

A new architecture for real-time image convolution with variable kernels is proposed. Due to computation flow transformation and memory-logic integration, we were able to exploit the excessive bandwidth inherent in memory and achieve the fine-grain parallelism of computations. Estimations show that the architecture is suitable for a real-time TV and HDTV picture convolution with very large kernels and can be implemented on a single VLSI chip.

MPA5 Equalization/Modulation/Decoding

Co-Chairs: Simone Fiori and Francesco Piazza

University of Acona

2:00 pm – 5:30pm - ***Room: Ferrante II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA5-1 -- Novel Reinitialization Method for Successive Blind Equalization of MIMO Communication Channel

Ma, Chor Tin and Yau, Sze Fong, *The Hong Kong University of Science and Technology*

This paper studies blind equalization problem in which the multi-input multi-output (MIMO) communication channels are to be equalized without any a priori knowledge. We modified a recently proposed sequential MIMO deconvolution algorithm and proposed a new reinitialization method for successive channel equalization. In the new approach, subsequently equalized channels will not suffer from degradation caused by errors in previous equalization. Simulation results confirmed the efficacy of the proposed method and all the channels are equalized with high quality.

MPA5-3 -- Narrow-Band Interference Rejection in OFDM-CDMA Transmission System

Hsiao, Hsu-Feng; Hseih, Meng-Han; and Wei, Che-Ho, *National Chiao Tung University*

In this paper, we present a new method called "differential threshold exciser (DTE)" to suppress narrow-band interference in OFDM-CDMA transmission system. Also, another threshold exciser, "over-through threshold exciser (OTTE)", is discussed. The two methods use different transform characteristics of the interference and information signal to suppress the narrow-band interference no matter the interference is stationary or nonstationary. The DTE algorithm has nearly the same performance with the OTTE algorithm with less computation complexity.

MPA5-4 -- BLADE: A New On-Line Blind Equalization Method based on the Burelian Distortion Measure

Fiori, Simone and Piazza, Francesco, *University of Ancona*

The aim of this paper is to present a new class of cost functions for Blind Channel Equalization said Generalized Distortion Measures, and to show a particular member of this class, the Burelian Measure, that recalls a cost firstly introduced by G. Burel in a Source Separation context. Here we derive a new blind equalization method we call BLADE, based on the above theory, and through simulations we show its usefulness in the Blind Equalization context.

MPA5-5 -- A Parallel Decoding Scheme for Turbo Codes

Hsu, Jah-Ming and Wang, Chin-Liang, *National Tsing Hua University*

The recursive computations in the MAP-based decoding of turbo codes usually introduce a significant amount of decoding delay. In this paper, we present a method for reducing the decoding delay by means of segmenting a block into several sub-blocks, which are partially overlapped. The proposed sub-block segmentation scheme allows for the parallel decoding of each component code by using several sub-block decoders. The number of steps for the recursive computations in each sub-block decoder is reduced to O(N/W), where W is the number of segmented sub-blocks. The decoding delay is approximately one Wth that of a conventional MAP-based turbo-coding system. The cost paid is a slight degradation in bit error rate performance and a reasonable increase in hardware complexity.

MPA5-6 -- Efficient Management of In-Place Path Metric Update and Its Implementation for Viterbi Decoders

Shieh, Ming-Der, Sheu, Ming-Hwa, Wu, Chien-Ming, and Ju, Wann-Shyang, *National Yunlin University of Science & Technology*

The in-place path metric scheduling is known as an efficient approach for sequential processing of the trellis, where the number of add_compare_select (ACS) units or processors is less than the number of states. In this paper, a systematic approach to partitioning a centralized memory into several banks to increase the memory bandwidth for in-place path metric update in Viterbi decoders is presented. Similar concepts can be extended to distribute the memory banks into ACS units if the ACS units are scheduled correspondingly to keep the interconnection minimal. Implementation results show that in terms of trade-off between hardware overhead and required memory bandwidth, an expected performance improvement can be achieved based on the proposed technique, especially for the trellis with a long constraint length.

MPA5-7 -- Three-Dimensional Equalization for the 3-D QAM System with Strength Reduction

Shalash, Ahmed F., and Parhi, Keshab K., *University of Minnesota*

Recently, the 3-D CAP system was introduced as a modification to the conventional 2-D CAP. This paper makes two contributions in the context of the 3-D CAP system. First, the QAM equivalent for the three-dimensional case is introduced by extending the 2-D complex notation into a 3-D vector notation. The definition is a modification of the well known quaternions. Second, the 3-D QAM filtering is redefined using algorithmic strength reduction to reduce the overall complexity by about one third with marginal degradation. The 3-D QAM system using 9 filters performs almost exactly as the 3-D CAP. Further complexity reduction is achieved by exploiting filtering reduction at the expense of only one dB of receiver SNR degradation.

MPA5-8 -- A New Polynomial Structure For Channel Equalization And ACI Suppression in 64-QAM Reception

Srivastava, M.C. and Saini, J.P., *Kamla Nehru Institute of Technology*

This paper presents a new multi-stage complex fractionally spaced bilinear perceptron (MCFSBLP) model for channel equalization and ACI suppression in 64-QAM reception. The model divides the task of equalizing M-QAM system into simple, fast and reliable subtasks in three stages, each with complexity not exceeding that of 40QAM. Simulation results show that 64-QAM can be reconstructed efficiently with slightly increased computations.

MPA 6 Circuit Techniques for Wireless Applications

Chair: Martin Snelgrove

Carleton University

2:00 pm – 5:30pm - ***Room: Ferrante III***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA6-1 -- A 1.8 GHz Subsampling CMOS Downconversion Circuit for Integrated Radio Circuits

Cijvat, Ellie and Eriksson, Patrik, *Royal Institute of Technology;* Tan Nianxiong, *Ericsson Components AB, (MERC)* and Tenhunen, Hannu, *Royal Institute of Technology*

A track- and hold-circuit has been designed, which can function as a subsampling mixer in the front-end of a receiver in a wireless communication handset. In a 0.6 mm CMOS-technology, two test chips have been made, one with the stand-alone mixer and one with an A/D converter integrated on the same chip. Measurement results show that the mixer is able to handle an input signal with a frequency of 1.8 GHz. The circuits operate with a single 5V supply.

MPA6-2 -- A CMOS Sampled-Data System for IF-to-Baseband Demodulation and Filtering

Baschirotto, Andrea, *University of Pavia*; and Denti, G. and Smori, C., *Politecnico di Milano*

A sampled-data SC network with undersampling technique has been used to frequency-shifting and filtering the FM signal at 10.7MHz. The system is composed by two blocks. The first block (sampled at 40.98MHz) rejects the image frequency for the second block which frequency-translates and filters the FM .signal. The system has been fully integrated in a 0.5µm CMOS technology and operates from a single 3V supply.

MPA6-3 -- 1.8 GHz CMOS LNA with On-Chip DC-Coupling for a Subsampling Direct Conversion Front-End

Parssinen, Aarno T.; Lindfors, Saska J; Ryynanen; Jussi H., and Halonen, Kari A, *Helsinki University of Technology*

A 1.8 GHz CMOS LNA, which is suitable as a front-end in a direct conversion radio receiver, has been designed. The LNA is designed to drive a capacitive load such as the load of a subsampling mixer. The output resonator limits the mixer input noise bandwidth, which is necessary to optimize the system noise figure. DC-coupling, an essential function in a direct conversion front-end, is realized with an on-chip structure, which has low sensitivity to parasitic effects. The LNA achieves NF of 3.4 dB and gain of 17 dB from 3 V supply.

MPA6-4 -- ASIC FOR 1-Ghz Wide Band Monobit Receiver

Pok, David and Chen, Henry Chien-In, *Wright State University*; Montgomery, C.; Tsui, B.Y.; and Schamus, John; *Wright-Patterson , AFB*

An ASIC for a wide band (1 GHz) digital monobit receiver designed for processing two simultaneous signals will be described. The receiver consists of three major elements: 1) a nonlinear radio frequency (RF) front-end, 2) a signal sampler and formatting system (analog-to-digital converter (ADC) and demultiplexers), and 3) a monobit algorithm implemented as an ASIC for signal detection and frequency measurement. The receiver uses a two-bit ADC operating at 2.5 GHz whose outputs are collected and formatted by demultiplexers for presentation to the ASIC.. The ASIC has two basic functions: 1) perform a fast Fourier transform (FFT) and 2) determine the number of signals and report their frequencies.

MPA6-5 -- RF Low-Noise Amplifiers

Martinez, Jose Silva, *INAOE* and Carreto-Castro, M.F., *National Institute of Astrophysics, Optics, and Electronics*

In this paper two Low-Noise Amplifiers (LNA) are presented. The first topology is a two-stage LNA that is ac coupled to the mixer, while the second one is a single stage LNA that can be dc coupled to the mixer.These circuits have small sensitivity to temperature variations and special biasing techniques allow us to reduce the effects of the process tolerances. Preliminary experimental results obtained from a prototype, not properly packaged for high frequency applications, have shown that the proposed technique works properly up to 250 MHz. These circuits have been fabricated in an 8 GHz 1.2 um BiCMOS technology

MPA6-6 -- A Low Power, Wide Linear-Range CMOS Voltage-Controlled Oscillator

Rhee, Woogeun, *Rockwell Semiconductor Systems, Inc.*

A low power CMOS voltage-controlled oscillator (VCO) is presented. Its simple and symmetric structure can provide low-power and low-noise operation, which is comparable to existing architectures in CMOS. The proposed VCO is digitally programmable to have different center frequencies while maintaining its linear voltage-to-frequency characteristic and a desirable VCO gain at tuned frequency. Simulation result shows that the output frequency of 1 GHz is achieved at the power consumption of 3.5 mW.

MPA6-8 -- A New GHz CMOS Cellular Oscillator Network

Moon, Gyu; Kim, Hong-Sun; Ismail, Mohammed; and Hwang, Changku, *The Ohio State University*

The design of a new CMOS Cellular Oscillator Network (CON) architecture is presented. With its simple cellular and fractal structure, this architecture can theoretically be spread in 2D or, possibly 3D with infinite number of feedback loops. Given a local disturbance from outside, these feedbacks, in turn, guarantee a uniformly distributed change in the global state as the network is based on the same cellular structure. Choosing the oscillation frequency as our state variable, and adopting a very high speed basic cell based on today's submicron CMOS technology, we present, in this paper, possibilities of using this architecture for GHz oscillators in RF communication systems. Potential benefits of this oscillator including accurate quadrature signal generation are discussed, and simulations in 0.5um CMOS are presented to verify the dynamics of this architecture.

MPA 7 Linear Circuits

Chair: Isao Shirakawa

Osaka University

2:00 pm – 5:30pm - ***Room: Bonzai I***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA7-1 -- Flow Problems on Information Network

Takatama, Hirokazu; and Watanabe, Hitoshi, *Soka University*

This paper presents a theory of information flow and new effective procedures of flow problems in large amount of information transmission for the cases of single source single sink (SSSS), single source multiple sinks(SSMS) and multiple sources multiple sinks (MSMS). Proposed distrbuted algorithms for SSSS and SSMS flow problems are executed by a parallel processing network PPN, the network with node-processors and the same topolgy as that of object network. For more general MSMS problem, a new method is proposed, where the algorithms of SSSS and SSMS problems are applied successively in time division manner. The significance of flow theory in information network is also discussed.

MPA7-2 -- Hybrid Matrix Minors from Tableau Applied to a MultiportGeneralization of NDR Related to Stability

Chaiken, Seth, *State University of New York, Albany*

Grassmann coordinates and a generalization of Cramer's rule are used to express every minor of every well-defined hybrid H or other description matrix of a linear t-ported network as a quotient of tableau minors. We give a multiple port generalization Green and Willson's theory that relates the sign of differential resistance of one inserted port to how the DC operating point potential stability changes when the (short or open) termination of the inserted port is changed. The determinant of the hybrid matrix H here generalizes resistance. Second, a universal topological formula for all the minors of H (and other descriptions) is given. Matroid theory simplifies some proofs.

MPA7-3 -- A Method For Automatic Design of Analog Circuits Based on a Behavioral Model

Shojaei, M.; and Sharif-Bakhtiar, M., *Sharif University of Technology*

A novel method for automatic synthesis of analog circuits is presented. A domain knowledge including circuit theory laws as well as circuit library and heuristics is used. The behavior and topological properties of the desired circuit is first derived. A behavioral graph with respect to the behavior of the basic components is then devised to match the behavior of the desired circuit. The behavioral model is then transformed to a corresponding circuit for an acceptable solution. These operations use algorithmic approaches for behavioral and topological modification based on KVL and KCL law. Consequently for a given design problem this method is able to produce different circuit topologies which do not necessarily exist in the library.

MPA7-4 -- Modified Nodal Formulation Method Applied to Piecewise-Linear DC Analysis

Roos, Janne Wilhelm; and Valtonen, Martti Erik, *Helsinki University of Technology*

The subject of this paper is piecewise-linear DC analysis based on modified nodal formulation. Two approaches to such an analysis are first developed. The elimination of the drawbacks of these analysis methods results in an efficient piecewise-linear DC analysis method that can be used to simulate general nonlinear circuits. The method proposed has been implemented in the APLAC circuit simulator.

MPA7-5 -- N-Port Reciprocity and Irreversible Thermodynamics

Weiss, Laurens and Mathis, Wolfgang, *Otto-von-Guericke-University Magdeburg*

The relation between the reciprocity of electrical networks and the thermodynamic Onsager-Casimir reciprocity is discussed, and the meaning of this relation for the theory of thermal noise in electrical networks is explained. Onsager-Casimir reciprocity is used in thermodynamic proofs of Nyquist's theorem for the description of thermal resistor noise. When a thermodynamic interpretation of electrical networks is given, the reciprocity of linear networks and Onsager-Casimir reciprocity are (basically) equivalent. Assuming certain restrictions on current controlled non-linear inductors and voltage controlled non-linear capacitors, this equivalence can be generalized to networks with non-linear dynamical elements. Onsager-Casimir reciprocity is a consequence of network reciprocity in case of non-linear networks, when only situations in the neighbourhood of equilibrium are considered. In non-linear systems, far from equilibrium, Onsager-Casimir reciprocity is not valid.

MPA7-6 -- NARX Approach to Black-Box Modeling of Circuit Elements

Maio, Ivano; Adolfo, Stievano, I.S.; Canavaro, F.G., *Politecnico di Torino*

This paper deals with the identification of NARX (Nonlinear AutoRegression with eXtra input) models for the numerical simulation of circuit containing nonlinear dynamic elements. NARX identification, based on a sequence of input/output samples, is useful for black-box modeling and for the refinement of models of nonlinear circuit elements. In order to assess the suitability of such an approach, we apply it to a CMOS inverter gate and experiment with the main elements controlling the identification process. We obtain accurate models with relatively simple structure and observe reliable operation of the identification process, as well as a good insensitivity to the noise content of the output samples. Such results confirm that NARX identification could be a useful tool for circuit simulations.

MPA7-7 -- A General Method of Feedback Amplifier Analysis

Nikolic, Borivoje, *University of California, Davis*; and Marjanovic, Slavoljub, *University of Belgrade*

A new method of feedback amplifier analysis is presented. The existing approaches to analysis and design of feedback amplifiers are either based on modeling of two-port amplifier and feedback networks or on calculating the return-ratio. These two approaches produce different results for the loop gain and return-ratio, and depending on circuit topology, can significantly differ in resulting closed loop gain. The new approach is based on the calculation of the return-ratio and the exact modeling of the amplifier without feedback. Resulting

expressions for the loop gain and the return ratio are equivalent. The method is algorithmic and gives the exact result for the closed-loop gain. Its application is general, straightforward, allows simple approximations and is suitable for hand analysis as well as for the computer-aided symbolic or numeric analysis. The method is verified on typical examples of negative feedback amplifiers.

MPA7-8 -- The Index of the Standard Circuit Equations of Passive RLCTG-Networks Does Not Exceed 2

Reißig, Gunther, *Technische Universitat Dresden*

Linear and nonlinear networks composed of independent sources, resistive, capacitive and inductive subnetworks, as well as ideal transformers and gyrators (RLCTG-networks) are investigated. Branches may be arbitrarily coupled within the resistive, capacitive and inductive subnetworks and these subnetworks may be non-reciprocal. It is shown that the tractability index of the standard circuit equations of such networks does not exceed 2, provided that the resistance, capacitance, and inductance matrices of the subnetworks are positive definite.

MPA 8 Continuous-Time Filters

Chair: Jaime Ramirez-Angulo

New Mexico State University

2:00 pm – 5:30pm - ***Room: Bonzai II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA8-1 -- Design of a CMOS Fully-differential Continuous-TimeTenth-Order Filter Based on IFLF Topology

Chiang, David, H., *Portland State University*

The design of a CMOS fully-differential continuous time tenth-order lowpass filter with equiripple group delay based on the inverse-follow-the-leader feedback (IFLF) topology is discussed. A very-high-frequency operational transconductance amplifier (OTA) with negative resistive load (NRL) is used as a basic building block. Simulation results show the group delay sensitivity of IFLF circuits is very large. Measurement results verify the design method of IFLF filters, and also their sensitivity problems. Solutions are proposed.

MPA8-2 -- A Sixth-Order UHF Bandpass Filter Using Silicon Bipolar Active Inductors

Roberts, Gordon W., and Leong, Choon Haw, *McGill University*

A novel design of a silicon all-NPN floating active inductor is presented. Using a 0.8 mm BiCMOS technology with the NPN fT's at 11GHz, inductance values in the range of 10 - 70 nH can be realized on-chip for filter applications in the UHF range. To illustrate the operation of this floating inductor, simulation and experimental results are provided for its application in a 6th-order elliptic LC bandpass filter.

MPA8-3 -- An Autozeroing Floating-Gate Bandpass Filter

Hasler, Paul *Georgia Institute of Technology*, and Minch, Bradley A., *Cornell University, and* Diorio, Chris, *University of Washington*

We have developed a bandpass floating-gate amplifier that uses tunneling and pFET hot-electron injection to set its DC operating point adaptively. Because the gate currents are small, the circuit exhibits a high-pass characteristic with a cutoff frequency less than 1 Hz. The high-frequency cutoff is controlled electronically, as is done in continuous-time filters. We have derived analytical models that completely characterize the amplifier and that are in good agreement with experimental data. This autozeroing floating-gate amplifier demonstrates how to use continuous-time, floating-gate adaptation in amplifier design.

MPA8-4 -- A Novel Loss Control Feedback Loop for VCO Indirect Tuning of RF Integrated Filters

Li, Dandan, *Columbia University*

A novel loss control loop for use in VCO indirect tuning systems of continuous-time filters is presented. In contrast to conventional schemes, this loop can achieve robust amplitude regulation.

MPA8-5 -- A 2V Low-Distortion CMOS Biquadratic Cell

Python, Dominique, *Swiss Federal Institute of Technology (EPFL)*

This paper presents a fully differential CMOS biquadratic cell using an active-C integrator at a 2V supply voltage. An operational transconductance amplifier is used based on grounded MOS transistors biased in the triode region by a simple current conveyor. The integrator do not require any additional input common-mode rejection circuit and has an inherent output common-mode stabilization circuit, making it very compact. The biquadratic cell shows a total harmonic distortion of -60dB for a 500kHz 1Vpp sinus signal. The power dissipation per pole is 300mW.

MPA8-6 -- Analysis of Noise and Interference in Companding Signal Processors

Krishnapura, Nagendra, and Tsividis, Yannis, *ColumbiaUniversity*, and Toth, Laszlo, *TKU,Budapest*

The analysis of the effects of noise and interference in companding signal processors are discussed. Important differences from the analysis and effects encountered in conventional signal processors are pointed out. Finally, the theoretical calculations are successfully compared to experimental results.

MPA8-7 -- Fundamental Limits to the Dynamic Range of Integrated Continuous-Time Integrators

Krishnapura, Nagendra, and Tsividis, Yannis, *ColumbiaUniversity*, and Toth, Laszlo, *TKU,Budapest*

We derive the fundamental limits of the dynamic range of integrated continuous-time integrators, for a given power consumption. We prove that the highest dynamic range is obtained with Miller integrators, and that Gm-C and Gm-Miller integrators exhibit similar performance.

MPA8-8 -- Impedance Scalers for IC Active Filters

Silva-Martínez, José, and Vázquez-González, Alejandro, *Instituto Nacional de Astrofísica,Optica y Electrónica*

Several impedance scalers for the implementation of IC active filters are proposed. The structures can be used for the spread reduction of the components in active filters. Also, the scaling up of capacitors and/or resitors make feasible the integration of large time constants. Although the proposed techniques are implemented by using MOS transistors better results should be obtained if BICMOS technologies are employed.

MPA 9 High Speed Communication Circuits

Chair: R. Jacob Baker

University of Idaho

2:00 pm – 5:30pm - ***Room: Bonzai III***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA9-1 -- A Phase Detector with No Dead Zone And a Very Wide Output Voltage Range Chargepump

Ahola, Rami, Halonen, Kari, and Routama, Jarkko, and Lindfors, Saska, *Helsinki University of Technology*

This paper discusses the effects of the so-called dead zone in the phase detector on the phase-noise behavior of phase-locked loop frequency synthesizers. A novel phase detector that completely overcomes this problem is introduced. Also, a chargepump with a very wide output voltage range is presented. This chargepump allows the use of a VCO with a wider tuning range and, thus, also a lower noise sensitivity. Measurement results that verify the proper operation of these blocks are also presented.

MPA9-2 -- A 150Mbit/S CMOS Clock Recovery PLL Including a New Improved Phase Detector and a Fully Integrated FLL

Routama, Jarkko, Antero, Koli, Kimmo, and Halonen, Kari, *Helsinki University of Technology*

This paper describes a 150Mbit/s clock recovery pll, which includes a new kind of phase detector. This phase detector has a compensation logic for the minimun phase difference, which improves the transfer function significantly. The circuit has also a separate frequency

locked loop to secure that the on-chip oscillator remains on the right locking range. The frequency loop is fully integrated and includes a digital oscillator control. the circuit has been designed with a standard 0.5um CMOS process.

MPA9-3 -- Low Noise Clock Synthesizer Design Using Optimal Bandwidth

Kim, Beomsup, Lim, Kyoohyun, and Park, Chan-Hong, ***KAIST***

This paper presents a salient method to design a low noise clock synthesizer for high-speed data processing applications. The proposed design method optimizes the loop bandwidth by using a discrete-time analysis of a PLL and minimizes the clock synthesizer output jitter. Computer simulation is performed and simulation results strongly support the theoretical analysis. A 900MHz clock synthesizer is experimentally designed and shows the minimum jitter at the optimum bandwidth obtained from the analysis.

MPA9-4 -- A Low Jitter 1.25GHz CMOS Analog PLL for Clock Recovery

Wu, Lin, and Black, William C., *Iowa State University*

Conventional PLL design techniques used to implement CMOS GHz range clock recovery circuits typically suffer from significant power supply coupled noise in large integrated systems. This noise worsens the jitter of the PLL and degrades the system Bit-Error-Rate (BER). This paper describes an analog approach which applies fully differential current steering technique throughout the whole PLL system in order to reject supply coupled noise. Moreover, since this circuit works at reduced voltage swing, it not only has the potential of operating at very high frequency but also dissipates less power at high frequencies than conventional CMOS logic. Simulation results show that this clock recovery circuit can work at 1.25GHz with power dissipation of less than 100mw. Jitter of the proposed structure is about 40% of that of digital single-ended PLL clock recovery circuits. All the simulations are based on HP 0.5um N-well CMOS single-poly triple-metal technology.

MPA9-5 -- A Modified Costats Loop for Clock Recovery and Frequency Synthesis

Amourah, Mezyad M., *Iowa State Uniersity.*

A clock recovery circuit that takes advantage of self biasing, and the presence of delayed and advanced versions of the VCO output to increase the phase detector gain has been designed and simulated using a 0.6mm CMOS N-well process. This clock recovery circuit shows a fast response time. In addition to clock recovery, this circuit can be used as a frequency multiplier or synthesizer, without additional circuitry. To reduce jitter, the feed back loop is closed only when there is a control signal to adjust the VCO frequency.

MPA9-6 -- Effects of Random Jitter on High-Speed CMOS Oscillators

Chen, Yiqin, and Geiger,Randall, *Iowa State University*

A comparison is made of the effects of device noise on the jitter of three different high-speed voltage-controlled ring oscillators. These comparisons show that oscillator architecture plays a significant role in jitter performance and that in high-speed oscillators, the device noise contributed when the MOS transistors are operating in the triode region is substantial. These comparisons also show minimal differences in the noise predicted by the simple and widely used noise model and that predicted by the more complete but more complicated model recently introduced by Sodini and Hellums

MPA9-7 -- A Novel Ring-Oscillator with a Very Small Process and Temperature Variation

Routama, Jarkko, Antero, Koli, and Kimmo, Kari, *Helsinki University of Technology*

This paper describes a new ring-oscillator circuit the conversion gain of which has only a 92% variation with all process variations over the temperature range of 0..100C. The operating range of the oscillator is 180..380mhz. the circuit uses a 3-stage ring-oscillator for low speed conditions and a 4-stage oscillator for high speed conditions. The division between low and fast conditions is based on the transconductance of the mos-transistors.Tthe oscillator has also a process and temperature dependent control current. Tthe circuit has been designed with a standard 0.5um cmos-process.

MPA9-8 -- Reduction of the 1/f Noise induced Phase Noise in a CMOS Ring Oscillator by Increasing the Amplitude of Oscillation.

Gierkink, Sander L.J.,*MESA Research Institute, Universityof Twente,*

Spectrum measurement results of a CMOS ring oscillator are presented that show a 10 dB decrease in 1/f noise induced phase noise at a 2 dB increase in carrier power. Simple ring oscillator theory predicts that the 1/f noise induced phase noise is independent of carrier power. It is shown that an increase in the amplitude of oscillation is accompanied by a reduction of the intrinsic 1/f noise of the periodically

switched MOS transistors in the ring. A net reduction of the 1/f noise of a periodically switched NMOS transistor of more than 12 dB is measured in baseband.

MPA 10 Interconnect Modeling and Design

Chair: Cem Goknar

University of Illinois

2:00 pm – 5:30pm - ***Room: San Carlos I***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA10-1 -- A Universal Closed-Loop High-Speed Interconnect Model for General Purpose Circuit Simulators

Li, X.; Nakhla, M.; and Achar, R., *Carleton University*

In this paper, a novel technique is presented for the computation of multiconductor transmission line stencils suitable for inclusion in general purpose circuit simulators such as SPICE. Transmission lines can be lossy, coupled and distributed. The method offers an efficient means to discretize transmission lines compared to the conventional lumped discretization. Coefficients of the approximation are computed using closed-loop Pad approximants of exponential matrices. The algorithm also provides an error criterion for automatically selecting the order of the approximation for the frequency-bandwidth of interest. Numerical examples are presented to demonstrate the validity of the proposed model and to illustrate its application to variety of interconnect structures.

MPA10-2 -- A Novel Technique for Minimum-Order Macromodel Synthesis of High-Speed Interconnect Subnetworks

Achar, R. and Nakhla, M., *Carleton University*

A new algorithm is presented to efficiently combine the process of model-reduction of high-speed interconect subnetworks with the nonlinear simulation. The proposed algorithm guarantees the number of states required during macromodel synthesis from reduced-order frequency-domain matrix-transfer functions to be minimum. This greatly speeds up the nonlinear simulation as the number of algebraic equations involved is reduced. An important advantage of the new technique is that it can be used in conjunction with any of the existing model-reduction techniques.

MPA10-3 -- Multipoint Multiport Algorithm for Passive Reduced-Order Model of Interconnect Networks

Yu, Qingjian; Wang, Janet M.L., and Kuh, Ernest S., *U.C. Berkeley*

In this paper, we prove that any real full-rank congruence transformation applied to a system of RLC interconnect described by MNA or state equations will result in a passive network, and provide an algorithm for multipoint multiport passive model-order reduction of RLC interconnect networks. The algorithm extends the matching points from real s-value to imaginary and infinity frequencies, and treats the moment matching for each port individually so that it is more flexible than the block-wise algorithms.

MPA10-4 -- Applications of Complex Frequency Hopping Method in PCB SignalIntegrity Simulation

Mu, Zhen, ***Cadence Design Systems, Canada***

This paper presents a fast Signal Integrity(SI) simulator using a newly published moment matching technique, Complex Frequency Hopping(CFH), which can effectively simulate boards containing a large number of interconnects with lossy parameters. For the first level examination of an entire board, this simulator provides an excellent solution to delay, reflection, and crosstalk by using linear component models. For the detailed analysis of an interconnection network with non-linear components, this simulator creates equivalent time domain macro-models to replace the linear subnetwork containing lossy interconnects. Such models can beeasily used in any SPICE like simulator to efficiently perform accurate time domain analysis of the network.

MPA10-5 -- Time Domain Method for Reduced Order Synthesis of Large RC Circuits

Batterywala, Shabbir Hussain and Narayanan, H., *Indian Institute of Technology, Powai*.

In this article we present a time domain method to approximate linear RC multiport networks, accurate up to user specified frequency. We use Lanczos algorithm to compute eigenvalues, an electrical network based method to compute eigenvectors and use these to synthesize a reduced order RC network. A similar method for RC multiport approximation has been proposed by Yang and Kerns which works with admittance matrices (G and sC) of the multiport and also uses Lanczos algorithm to compute dominant eigenvalues and eigenvectors. However their method forbids capacitor cutsets in the multiport, which is a common occurrence in multilayered interconnect modeling, signal integrity analyses etc. We propose an algorithm which works implicitly on the state matrix description of the network and allows capacitor cutsets in the graph of the network. We use an efficient DC analysis algorithm to make implicit computations of eigenvalues, eigenvectors and port admittance matrices.

MPA10-6 -- CMOS Inverter Current and Delay Model Incorporating Interconnect Effects

Hafed, Mohamed and Rumin, Nicholas, *McGill University*

We present a new model for predicting the switching current and delay in a CMOS inverter with an RC load. The model exploits the ability of an inverter model such as the one described in [1] to predict accurately the current peak time, tm, as a function of inverter size, input slope and capacitive load. An iterative procedure computes the effective capacitance presented by the RC load, using an empirical model for the output voltage of the RC load driven by a

reference inverter. Not only is the resulting model accurate but computationally efficient as well, so that the two to three order speed up over HSPICE achieved in [1] is preserved.

MPA10-7 -- Path Resizing Based on Incremental Technique

Cremoux, Severine; Azemard-Crestani, Nadine; and Auvergne, Daniel; *LIRMM*

Based on an incremental path search algorithm, this paper addresses the problem of longest combinational paths selection for performance optimization at physical level. A realistic evaluation of gate delay and controlled sizing techniques are used to manage the circuit path sizing alternatives, such as delay or power/area constraints. The efficiency of this technique is demonstrated and also illustrated on several ISCAS'85 benchmark circuits. A comparison is given between regular sizing alternatives to local optimization steps controlled by specific indicators.

MPA10-8 -- Substrate Coupling Analysis and Simulation for an Industrial Phase-Locked Loop

Welch, Ryan Joseph and Young, Andrew T., *University of Washington*

Current injected into the common chip substrate from fast-switching digital devices can affect the operation of sensitive analog circuits in mixed signal designs. An industrial Phase-Locked Loop(PLL) is analyzed with the non-ideal substrate modeled to show the effects of substrate coupling. Detailed simulation results strongly correlate to the measured circuit jitter. Additional results show that well guard structures should not be used and the effectiveness of ohmic guarding structures depends on number, location in the layout, and the bias scheme.

MPA 11 Multi Sensor Data Fusion: Application and Issues

Chair: Sean Midwood

Canadian Navy *Special Session*

Organizer: Sean Midwood

Canadian Navy

Ian Glenn

Canadian Army

2:00 pm – 5:30pm - ***Room: San Carlos II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA11-1 -- An Introduction to Multi-Sensor Data Fusion

Llinas, James, *State University of New York at Buffalo* and Hall, David L., *Pennsylvania State University*

Multi-sensor data fusion is an emerging technology applied to Department of Defense (DoD) areas such as automated target recognition, battlefield surveillance, and guidance and control of autonomous vehicles, and to non-DoD Applications such as monitoring of complex; machinery, medical diagnosis, and smart buildings. Techniques for multi-sensor data fusion are drawn from a wide range of areas including artificial intelligence, pattern recognition, statistical estimation, and other areas. This paper provides a tutorial on data fusion, introducing data fusion applications, process models, and identification of applicable techniques. Comments are made on the state-of-the-art in data fusion.

MPA11-2 -- From GI Joe To Starship Trooper: The Evolution of Information Support for Individual Soldiers

Llinas, James, *State University of New York at Buffalo* and Hall, David L., *Pennsylvania State University*

As we approach the millennium, numerous programs and research plans have focused on the use of advanced technology to improve the effectiveness of military forces. Examples include: the Army XXI concepts and the Army After Next (http://cacfs.army.mil/aan.html) concepts for military technology beyond the year 2020. Technologies to improve the effectiveness of soldiers include advanced tactical communications, the Global Positioning Satellite (GPS) system for precise geolocation, fire and forget smart weapons, improved sensor, and multi-sensor data fusion systems. The interest in such technology is exemplified by the recent movie, Starship Troopers, based on a science fiction book by Heinlein[9]. This paper summarizes come of the innovations provided to soldiers to transform them from the era of GI Joe to an anticipated era of the starship trooper. In particular, we analyze information technologies such as advanced sensors, multi-sensor data fusion, and automated reasoning.

MPA11-3 -- A Multisensor Data Fusion Algorithm for the USCG's Vessel Traffic Services System

Glenn, Ian N., *Department of National Defence, Canada*

This paper describes the development of an algorithm to fuse redundant observations due to multiple sensor (type and location) coverage in order to provide a significant reduction in duplicate track information provided to Vessel Traffic Services (VTS) operator displays. The design of the algorithm allows acceptance of inputs from any type of sensor (radar, acoustic, GPS, system generated and manual tracks) as long as the basic decision criteria elements are provided. The result of this effort is a computationally efficient and cost effective software solution to a significant system deficiency that impacts greatly on overall waterway safety. The algorithm is tested with real data collected from the VTS system at Puget Sound in September 1996.

MPA11-5 -- Microsimulation as a Tool for Target Tracking and State Estimation

Brown, Donald E. and Pittard, C. Louis, *University of Virginia*

Data fusion systems process large amounts of data into information for decision support. One of the fundamental components of data fusion is state estimation which provides estimates of current and future environmental states. Traditionally the state estimation procedures in data fusion have been accomplished by Kalman filtering techniques. However, these methods have difficulties with domains such as ground operations where past behavior does not correlate as highly with future behavior. This paper provides an overview to the use of microsimulations for state estimation in this domain.

MPA11-6 -- Information Understanding: Integrating Data Fusion and Data Mining Processes

Waltz, Edward, *ERIM International*

Data fusion and data mining are complementary processes that contribute abductive-inductive (learning and discovery) and deductive (detection) capabilities. Not to be confused with each other, the processes offer distinct and reciprocal capabilities that, once integrated,

provide powerful tools for improving the automatic recognition of targets by complex, non-literal signatures from multiple sources. ERIM International is developing and applying this integrated technology to improve the performance of traditional data fusion processes.

MPA11-8 -- Strategically-Controlled Information Fusion

Flank, Steven M., *Defense Advanced Research Projects Agency (DARPA)*

Core Approach for Strategically Controlled Information Fusion Define performance metrics that quantitatively characterize fusion engine (FE) output. Define context metrics that quantitatively characterize FE performance as a function of input data. Quantitatively map FEs' performance space (how predicted performance depends on context). Encapsulate FEs so that they share data representations, services, and queries. Control this confederation of encapsulated FEs with an intelligent fusion strategist that maximizes overall performance as a function of context by: a) Selecting the FE with the best-predicted performance for a given real-time context; b) Sequencing FEs to maximize performance by receiving data sets outputs from other FEs, thus improving the region of the performance space in which they operate; c) Adjusting FE control and modeling parameters to achieve peak performance over a broader range of contexts; d) Reacting to FE outputs by comparing to predicted performance and adjusting parameters, sequences, and selections to maintain overall performance.

MPA11-9 -- The CANADA-NETHERLANDS Collaboration on MultiSensor Data Fusion and Other Canada-NATO MSDF Activities

Bosse, Eloi; Roy, Jean; and Bosse, Eloi, *Canada National Defence*

This paper describes a collaborative effort between Canada and The Netherlands in analyzing multi-sensor data fusion systems. In view of the overlapping interest in studying and comparing applicability and performance of advanced state-of-the-art Multi-SensorData Fusion (MSDF) techniques, the two research establishments involved (DREV and TNO/FEL) have decided to join their efforts in the development of MSDF testbeds. This resulted in the Joint-FACET (Fusion Algorithms & Concepts Exploration Testbed), a highly modular and flexible series of applications that is capable of processing both real and synthetic input data. In addition to the bilateral collaboration with The Netherlands, this paper presents a survey of the other Canadian MSDF activities conducted under NATO Research Study Groups.

MPA 12 Power Distribution Systems

Chair: David A. Johns

University of Toronto

2:00 pm – 5:30pm - ***Room: San Carlos III***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA12-1 -- A Power Distributor with Winner-Take-All Function

Mokunaka, Naoki; and Saito, Toshimichi, *Hosei University*

This paper proposes a novel power distributing system with winner-take-all function. The dynamics can be comprehended by an N-dimensional return map described by piecewise exact solutions. We have clarified that the system exhibits various interesting periodic phenomena as load distribution varies, e.g., Cantor-function-like duty and current characteristics.

MPA12-2 -- A DSP Controlled Variable Frequency Resonant-Commutated Converter

Chickamenahalli, Shamala A.; Liu, Jon; Nallapervimal V.; and Barker, Clashow M., *Wayne State University*

The features of a three-phase resonant-commutation based variable-frequency converter applicable in a variety of industrial applications are presented. Minimization of switching losses as accomplished by resonant commutation of the converter is highlighted. Design and development of the DSP based controller is described. Strategies developed for switching of converter devices in relation to the resonant-commutated link are discussed. Results from Pspice simulation studies of the converter are presented. Experimental results while the single-phase laboratory model of the converter supplied passive loads are enclosed and observations summarized.

MPA12-4 -- New Parallel Tabu Search for Voltage and Reactive Power Controlin Power Systems

Mori, Hiroyuki; and Hayashi, Takanori, *Meiji University*

This paper proposes a new method for voltage and reactive power control in power systems. The proposed method is based on tabu search that is effective for combinatorial problems. Tabu search makes use of the idea of the hill-climbing method, but some search directions are fixed to escape from local minima. To improve the solution accuracy, a parallel scheme for tabu search is developed so that the

neighborhood is computed in a parallel way with different tabu lengths. In this paper, the proposed method is applied to voltage and reactive power control in power systems. The efficiency of the proposed method is demonstrated in a sample system.

MPA12-5 -- Power Energy Metering Based on Random Signal Processing (EC-RPS)

Toral, Sergio L.; Quero, Jose Manuel; and Franquelo, Leopoldo, *INGENIEROS*

The monitoring of electrical energy consumption achieves better performances using static counters. However high quality systems using DSP provide very accurate measurements, but with a high cost. On the other hand, cheap devices are not very accurate.In this paper we propose the use of stochastic signal processing to implement static energy counters. The simplicity of the digital circuits utilizing this technique allows for the calculation of electrical measurements. We propose digital circuits for computing the active and reactive energy consumption and power factor for mono-phase and poly-phase systems. The results of an active power meter implemented using an FPGA device are compared to the ones obtained using a commercial analyzer.

MPA12-6 -- Sensitivity Analysis of Power System Trajectories: Recent Results

Hiskens, Ian A. and Pai, M.A., *University of Illinois at Urbana-Champaign*

The development of trajectory sensitivity analysis for power systems is presented in the paper. A hybrid system model which has a differential-algebraic-discrete structure is proposed. Crucial to the analysis is the development of jump conditions describing the behaviour of sensitivities at discrete events, such as switching and state resetting. A power system example which involves a mix of continuous and discrete behaviour is presented to illustrate various aspects of the theory. It is shown that trajectory sensitivities provide insights into system behaviour which cannot be obtained from traditional simulations.

MPA12-7 -- Contingency Screening Using Interval Analysis in Power Systems

Mori, Hiroyuki; and Yuihara, Atsushi, *Meiji University*

This paper proposes a contingency screening method for considering uncertainty with interval analysis that may expresses a variable as an interval number or the lower and upper bounds. The proposed is used to handle uncertainty of nodal voltage variables that stems from the variation of the nodal injection powers. The linearized power flow equations is considered as a basis of contingency screening. This paper focuses on the interval Gauss-Seidel and the simple iteration methods a method for interval analysis in the linear equation. The methods are applied to sample systems. A comparison between them is made to examine the performance in terms of solution accuracy and computational effort.

MPA12-8 -- Estimation of Nonsinusoidal Bus Voltage Wave Forms in Power Systems

Abur, Ali, *Texas A&M University*

This paper presents a method of estimation of nonsinusoidal bus voltage waveforms in power systems. Harmonics associated with bus voltages of interest are subsequently calculated. Power system is modeled using discrete time models of elements and the corresponding measuremenet equations are derived. A recursive least squares estimation algorithm is used to track the system voltages in discrete time. Performance of the algorithm is evaluated by simulations on a sample power system.

MPA 13 Image and Video Processing I Poster Session

Co-Chairs: Ya-Qin Zhang and Oscar Au

Saroff Corporation and Hong Kong University of Science and Technology

2:00 pm – 5:30pm - ***Room: Serra Ballroom Back I***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA13-1 -- A Multi-Transform Approach to Reversible Embedded Image Compression

Adams, Michael David and Antoniou, Andreas, *University of Victoria*

Several reversible wavelet transforms known to work well for image compression are introduced, and the classes of images for which the various transforms are effective are described. Then a multi-transform approach to reversible embedded image compression is proposed in which the decorrelating transform is selected on a per image basis using image-specific characteristics. Although the selection algorithm is extremely simple and has only modest computational requirements, results show that this new approach yields better compression performance than is possible with the use of a single fixed transform such as the S+P transform.

MPA13-2 -- Dynamic Load Balancing for Distributed Movie Based Browser Systems

Hiraiwa, Atsunobu; Komatsu, Naohisa; Komiya, Kazumi; and Ikeda, Hiroaki, *Telecommunications Advancement Organization of Japan*

This paper describes the dynamic load balancing of distributed movie based browser systems, which can visually be navigated by the integration of movies and linking-information. The linking-information indicates replicated multimedia information (such as sounds, videos and multiple super high definition (SHD) pictures) stored in each server on the network. Proposed new dynamic media partitioning performs the load-balancing of the respective server and network for multimedia information. The proposed method efficiently uses the servers and network, reserving and allocating the bandwidths of the transmission lines between a client and servers on the network, monitoring the load on each server, and effectively partitioning continuous multimedia information. This method provides a solution to the problem caused by lack of the bandwidths that the server supplies to the client, or by lack of the bandwidths of the transmission lines between a client and a server on the network. The problem is derived from the deficiency of the throughput (64Mbit/s) for lines with required high bandwidths (192Mbit/s), long delay times (the round-trip time measures 8 ms) and a window size of 64Kbytes. Improved dynamic media partitioning including a round-trip time parameter provides high throughput of 192Mbits/sec by partitioning and allocating the load to 3 servers, giving a solution to this problem.

MPA13-3 -- The Impact of Encoding Algorithms on MPEG VLSI Implementation

Cheng, Sheu-Chih and Hang, Hsueh-Ming, *NCTU*

The goal of this paper is to study the impact of MPEG encoding algorithms from a system-level design viewpoint. An area-time estimation tool is developed to extract the timing requirement and silicon area for various combinations of hardware modules and algorithms. After complemented the design of several modules in an MPEG encoder, we found that the motion estimation and rate control modules consume most part of the silicon area in the encoding chip. We also evaluated the entire chip area of a few cases for two picture formats. The methodology and results presented here should provide useful guidelines in selecting an appropriate MPEG encoding algorithm for VLSI design.

MPA13-4 -- Efficient Subtree Splitting Algorithm for Wavelet-based Fractal Image Coding

Po, Lai-Man, *City University of Hong Kong*; Zhang, Ying, *Guangdong Posts & Telecommunications*; Cheung, Kwok-Wai and Cheung, Chun-Ho, *City University of Hong Kong*

In this paper, a novel wavelet subtree splitting algorithm is proposed, which divides a subtree into scalar quantized wavelet coefficients and fractal coded sub-subtree. Based on this new technique, a variable size wavelet subtree fractal coding scheme for still image compression is developed. Experimental results show that the new scheme can achieve nearly optimal partition of wavelet subtree with substantially computational reduction as compared with Davis' scheme.

MPA13-5 -- Error Resilient Image Coding with Rate-Compatible Punctured Convolutional Codes

Cai, Jianfei and Chen, Chang Wen, *University of Missouri-Columbia*; and Sun, Zhaohui, *University of Rochester*

In this paper, we describe an application of the rate-compatible punctured convolutional (RCPC) channel codes to an error-resilient image compression scheme with variable-coefficient fixed-length (VCFL) source codes. The VCFL source coder is error resilient because of its fixed length of the codes. Since it is based on wavelet transform, the scheme provides us with a hierarchical structure of the source codes to facilitate the unequal error protection by the channel codes. We adopt the RCPC codes for channel coding to achieve three goals: (1) Unequal error protection, (2) single channel decoder with multiple rate compatibility, (3) minimizing controlled overhead redundancy. Iminary results show that, with slightly higher bit rate, we can achieve better ucted image quality under at least an order of magnitude higher channel bit error rate.

MPA13-6 -- Fast Motion Estimation Based on Total Least Squares for Video Encoding

Deshpande, Sachin G. and Hwang, Jenq-Neng, *University of Washington*

In this paper a new fast motion estimation method useful for video encoding in a noisy environment is presented. Motion estimation methods can broadly categorized as Block Matching (BM) methods, Pel Recursive (PR) methods, and Frequency Domain (FD) methods. Majority of the current fast motion estimation methods belong to block matching category. These methods typically achieve speedup by either reducing the number of search locations or by reducing the number of computations at each search location.. Our proposed method is based on the pel recursive formulation. However, in order to achieve fast estimation, we operate on a block of pixels. To provide a robust behavior in a noisy environment we use a Total Least Squares (TLS) based estimation scheme which aims at estimating the true motion vectors. The simulation results indicate the speedup and robustness of the algorithm in noisy environment.

MPA13-7 -- Error Control for H.263 Video Transmission over Wireless Channels

Chen, Yen-Lin and Lin, David W., *National Chiao Tung University*

We consider ways to combat the error effects when transmitting H.263 video over a wireless channel. The error control measures consist of two "layers," namely, that of the coded bitstream and of the video information. At the bitstream layer, we employ error-resilient entropy coding (EREC), with pseudo-random block interleaving, to reduce the error propagation in decoding of variable-length codewords. At the information layer, we employ a DC recovery scheme to conceal the effects of corrupted DC coefficients. Corrupted motion vectors are detected and corrected using a motion-vector pairing technique in the encoder and a corresponding motion-vector checking and recovery algorithm in the decoder. By these methods, corrupted strips in the images caused by loss of synchronization are avoided. The annoying "green/pink block artifacts" caused by erroneous DC coefficients and the effects of incorrect motion compensation caused by corrupted motion vectors are also reduced.

MPA13-8 -- Comparison between Block-based and Pixel-based Temporal Interpolation for Video Coding

Tang, Chi Wah and Au, Oscar C., *HK University of Science & Technology*

In very low bit rate (VLBR) video conferencing and videotelephony applications, the bit rate of sending video sequences must be kept low due to the limited channel bandwidth. To satisfy the VLBR requirement), temporal subsampling is a simple technique which may be combined with other compression schemes to achieve very large compression ratio. A previous proposed block-based motion compensated temporal interpolation (MCTI) [1-3] can interpolate frames with reasonably good visual quality but also with some blocking artifacts. In this paper, the block based MCTI is compared with a pixel-based approach. While the pixel-based approach has good performance in some test cases, it is highly computationally intensive making it rather unpractical. It is also found to perform poorly in some sequences.

MPA13-9 -- A Scalable Hierarchical Motion Estimation Algorithm for MPEG 2

Song, Xudong; Chiang, Tihao, and Zhang, Ya-Qin, *Sarnoff Corporation*

In this paper, a new scalable hierarchical motion vector estimation algorithm is developed for MPEG-1 and MPEG-2 encoder applications. The scalable hierarchical motion estimation architecture uses a 4-layer pyramid switching from one-bit/pixel to eight-bit/pixel representation according to the available platform resources and/or user's choices. The scalability is realized in terms of computational complexity, memory requirement and communication bandwith. Four picture quality levels correspond to four complexity levels. With such features, platform-adaptive e ncoding and computing is made possible.

MPA13-10 -- Transform Domain Motion Estimation without Macroblock-based Repetitive Padding for MPEG-4 Video

Chen, Jie and Liu, K.J. Ray, *University of Maryland*

In order to perform motion estimation and compensation (ME/MC) of an arbitrarily shaped video object plane (VOP), macroblock-based repetitive padding is applied to the blocks on the borders of the reference VOP of MPEG-4 video. However the padding undesirably increases the overall complexity and data flow. In this paper, we propose transform domain motion estimation without repetitive padding for MPEG-4 video. It directly extracts motion vectors out of the two consecutive VOPs of the moving object. The resulted approach has low computational complexity compared to the modified block (polygon) matching motion estimation (MBKM-ME) in MPEG-4 video verification model (VM). Most importantly, the DCT-based nature enables the combination of both DCT and motion estimation units, thus the simplification of the heavily loaded feedback loop in MPEG-4 video coder design. It leads to a low-complexity, high-throughput fully DCT-based video coder. Moreover the proposed algorithm has inherently massive parallel operations and local connections suitable for VLSI implementation. Simulation demonstrates comparable performance of our transform domain approach and MBKM-ME in MPEG-4 video VM in terms of prediction errors.

MPA13-11 -- Using a Region-Based Blurring Method and Bits Reallocation to Enhance Quality on Face Region in Very Low Bitrate Video Coding

Chen, Chang-Hung; Chen, Liang-Gee; and Chang, Hao-Chieh, *DSP/IC Design Lab.*

A region-based blurring algorithm to reduce bitrate in very low bitrate video coding is proposed. This algorithm reduces the bitrate by passing the original background image through a filter before motion estimation. Each frame in original sequence will be segmented into foreground and background at first. Background part, which is of less importance for human vision, will be blurred through a blurring filter, while the foreground is kept unchanged. The bitrate for head-and-shoulder type sequences can achieve 5%~20% bitrate saving by this blurring algorithm. According to the human vision model, PSNR degradation in the background is not evident. Using this blurring algorithm, but kept coded bitstream the same bitrate with the original sequence, about 0.5~1dB gain in foreground can be achieved due to bits reallo-cation between foreground and background.

MPA13-12 -- A Novel and Fast Feature Based Motion Estimation Algorithm Through Extraction of Background and Object

Mok, Wai Hung and Yung, Hon Ching Nelson, *The University of Hong Kong*

This paper presents a novel and fast Feature Based Motion Estimation algorithm which is developed for typical video-phone scenario. In essence it combines the technique of object extraction with traditional block based motion estimation methods by estimating the background and extracting the moving object continuously in the first stage, then performs a block based motion estimation on the extracted. Simulation of the algorithm with full search as core shows that the estimation time can be reduced by as much as 50%, while the MSE and PSNR remain almost the same as the full search results.

MPA13-13 -- An Adaptive Arithmetic Coding Method Using Fuzzy Logic and Gray Theory

Jou, Jer Min and Chen, Pei-Yin, *National Cheng Kung University*

This paper describes an adaptive arithmetic coding method using a fuzzy gray tuner for on-line data compression. It is simple and suitable for hardware implementation, and can achieve high coding throughput. Compared with other schemes', the compression results of our method are good and satsifactory no matter what kind of source data is.

MPA13-14 -- An Integrated Classifier in Classified Coding

Huang, Jiwu, *New Jersey Institute of Technology;* Chen, Li, *Shantou University*; and Shi, Yun Q., *New Jersey Institute of Technology*

Block coding is one of the most common schemes in image data compression. To improve the performance of block coding, a classification can be applied to the blocks prior to coding. This results in an adaptive block coding method, i.e, classified coding. In this paper, an integrated classifier taking the features of the human vision system (HVS) into account in classified coding is proposed. First, we present a classifier based on the local contrast sensitivity of the HVS. Compared with the commonly used local variance-based classifier (LVC), it possesses lower computational complexity while preserving almost the same performance. To improve upon the single-parameter classifiers' poor adaptivity , we, then, propose an integrated classifier which is composed of three independent classification units. It exhibits the complementarity of different classifiers. The simulation results demonstrate that the proposed classifier performs better than the LVC.

MPA13-15 Corner Detection using Gabor-Type Filtering

Quddus, Azhar and Fahmy, Moustafu, *King Fahd University of Pet. and Minerals*

In this paper a new corner detection technique using Gabor filters is proposed. It is suitable for both binary and gray level images with varying backgrounds. This technique is based on scale interaction model, where the difference of two lowpass filters (with different bandwidths) is utilized to extract the corners, line intersections and line endings in the input image. The filtering is done iteratively until the change in the output is below a certain threshold. This technique does not require tracking the boundary and computing the curvature. The important features of the scheme include simplicity, robustness, speed of processing and availability of simple controls to tune the technique for various computer vision applications.

MPA13-16 Detection of Vehicle Occlusion Using a Generalized Deformable Model

Yung, H. C. Nelson and Lai, Hon Seng, *The University of Hong Kong*

This paper presents a vehicle occlusion detection algorithm based on a generalized deformable model. A 3D solid cuboid model with up to six vertices is employed to fit any vehicle images, by varying the vertices for a best fit. The advantage of using such a model is that the number of parameterized vertices is small which can be easily deformed. Occlusion is detected by recording the changes in the Area Ratio and the dimensions of the generalized deformable model. Our tests show that the new modeling algorithm is effective in detecting vehicle occlusion.

MPA13-17 Error Resilient Coding for JPEG Image Transmission over Wireless Fading Channels

Chandramouli, Rajarathnam, *University of South Florida,*

In this paper ,a new fast error resilient entropy coder (FEREC) for robust image transmission over wireless fading channels is proposed. A slow, frequency non-selective Rayleigh fading channel model is used. The FEREC algorithm is observed to be almost twice as fast as EREC proposed by Redmill et al. in encoding the data and hence the error resilience capability is also significantly better. Up to 2 dB improvement in the peak signal to noise ratio of the received image is achieved when compared to EREC.

MPA13-18 Noise Sensitivity Analysis for a Novel Error Recovery Technique

Hasan, Moh'd Abdel Majid, *AMIEE* and Marvasti, Farokh I., *King's College, MIEEE*

Many error correction codes and error recovery techniques have been developed to recover bursts of errors. Some of these codes are very robust and can recover the missing samples when a signal is transmitted via a noisy channel. The protected codewords sent to the receiver are subject to quantization noise due to the quantization of the protected samples. Also, these codewords suffer from degradation due to the additive channel noise. A robust burst error recovery technique similar to the Reed Solomon (RS) algorithm is presented in this paper with a comprehensive study of the sensitivity of this technique to quantization and additive white noise.

MPA13-19 On the Perceptual Interband Correlation for Octave Subband Coding

Liu, Chi-Min and Wang, Chung-Neng, *National Chiao Tugn University*

The ability of human vision systems to distinguishing gray values of pixels depends on factors such as background luminance, the nearby image contents, etc. Thus, for any image, there are various representations subjectively judged to be the same with the original. This subjective phenomenon provides the conjecture that some of the various representations may provide the statistical interband correlation instead of just the perceptual similarity with the original image. This conjecture motivates the work to exploit the desired representations and check the associated new merits. This paper demonstrates that the most desired representation can be systematically exploited such that the interband correlation of octave subbands is increased. We present two methods with different complexity and show the resultant coding gains. The gains indicate that there exist amounts of perceptual correlation applicable to image coding despite that the original interband correlation has been considered low.

MPA13-20 Analyzing Memory Bandwidth Requirements of Video Algorithms

Kapoor, Bhanu, *Texas Instruments Incorporated*

Memory bandwidth is emerging as the fundamental impediment to higher performance and lower power computer and communication systems. In this paper, we present an analysis of memory bandwidth requirements for the H.263 video codec algorithms. We make use of memory traces generated as a result of running Telenor's H.263 video encoder and decoder software implementations to simulate a large number of cache configurations. In the area of analysis of video algorithms, this paper focuses on the following issues: We provide a study of how varying cache size, block size, associativity, replacement policy and organization parameters such as split versus unified cache affects memory bandwidth requirements. A comparative study of encoder and decoder bandwidth requirements is presented. We also study various advanced encoding options provided with the H.263 standard in this light. Based on our study, we provide guidelines for the traffic-directed memory system design.

MPA13-21 An Adaptive Network Control Scheme for Region-Based Hybrid Coding Algorithm

Chen, Hsu-Tung, Chen, Liang-Gee, Huang, Sheng-Chieh, Tsai, Tsung-Han and Chang, Hao-Chieh, *National Taiwan University*

Based on the packet loss rate and the frame loss rate experiment in the practical Internet environment, a novel adaptive network control scheme is proposed for region-based hybrid coding algorithm. In comparison with the source/channel coding [1], this adaptive network control scheme is presented to reduce 50% frame loss rate during the Internet weak day use condition and 58% frame loss rate during the Internet peak day use condition.

MPA13-22 -- On Piecewise-Quadratic Filter for Gaussian Noisy Image Filtering

Li, Wenzhe; and Lin, Ji-Nan; and Unbehauen, Rolf, *University Erlangen-Nuernberg*

Image classification according to features or a statistical property relates often to a partition of the image domain space. Such a partition concept used in image filtering suggests that a nonlinear filter with a piecewise property is a suitable candidate. In this paper, we propose a novel kind of nonlinear filter, the piecewise-quadratic (PWQ) filter for Gaussian noisy image filtering, which utilizes the domain partition property in the filter function for various image features. We show that after a proper training of the filter function, such a filter has a good noise smoothing as well as an effective edge/detail-preserving property. Simulations are carried out for natural images and two examples are given for showing the performance of the proposed filter.

MPA13-23 MPEG-4 Accelerator for PC Based Codec Implementation

Lim, Young-Kwon; Kwak, Jinsok; and Park, Sanggyu, *Electronics and Telecommunications Research Institute*

In the MPEG-4 world, a scene is described as a composition of independent audiovisual objects that the user can access and manipulate. The MPEG-4 video being currently standardized will provide a toolbox containing tools and algorithms brining solutions enabling functionality. So it is very difficult to satisfy the various MPEG-4 video requirements using dedicated hardwares. In this paper we propose a flexible and high performance hardware architecture using DSP in conjunction with an MEMC (Motion Estimation and Motion Compensation) ASIC chip to implement MPEG-4 video codec. We developed the MEMC chip for an MPEG-2 MP@ML encoder. In order to see if it is possible to adopt the MEMC chip for the MPEG-4 accelerator, we simulated a modified MPEG-4 Video VM (Verification Model). The results of computer simulation showed that we can adopt the MEMC chip to implement MPEG-4 video.

MPA13-24 Rate Control in Video Coding by Adaptive Mode Selection

Ryu, Chul, *Polytechnic University*; and Kim, Seung, *InterDigital Telecommunication*

This paper presents an effective rate control algorithm by adaptively selecting the optimal modes for macroblocks in a block based video coder. For a given frame, the optimal modes are selected based on a decision curve that minimizes the overall distortion for a given bitrate. The proposed approach is different from the previous ones in that it does not manipulate quantizer to meet target bitrate. Instead it controls the decision curve to meet that target bitrate. The curve is obtained by utilizing simulated annealing optimization technique. The algorithm is implemented within H.261 video codec and simulation results are compared with other approaches.

MPA 14 VLSI I — Poster Session

Chair: Igor Filanovsky

University of Alberta

2:00 pm – 5:30pm - ***Room: Serra Ballroom Back II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA14-1 A Pulse-Triggered TSPC Flip-Flop for High-Speed Low-Power VLSI Design Applications

Wang, Jinn Shyan and Yang, Po-Hui, *National Chung Cheng University*

A new fast low-power flip-flop, called pulse-triggered TSPC flip-flop (PTTFF), is proposed. PTTFF uses a conventional latch
structure clocked by a short pulse train, and it indeed acts as a flip-flop. The new flip-flop uses only 5 MOS transistors with only one transistor being clocked. Both the total transistor count and the number of clocked transistors per flip-flop are reduced to save the power consumption of the flip-flop itself and the clocking system. For a pipelined FIR macro, utilizing the proposed PTTFF can save up to 63% of power consumption of the clocking system. PTTFF can also operate very fast. The maximum toggle rate of PTTFF can be as high as 3GHz if designed in a 0.6um CMOS technology.

MPA14-2 -- A Programmable Interpolation Filter for Digital Communications Applications

Kuo, Tzu-Chieh; Kwentus, Alan, and Willson, Jr., Alan N., *UCLA*

The design, implementation and testing of an interpolation filter IC suitable for digital BPSK and QPSK communications applications is discussed. The multiplierless filter consists of a 41-tap programmable interpolate-by-four pulse-shaping filter and a CIC (cascaded integrator and comb) filter whose interpolation ratio can be any integer between two and 1024. Several techniques such as polyphase decomposition for multirate systems and DC gain compensation schemes are exploited so that both high speed and low power consumption can be achieved with simplified structures. Simulation and test results show this 0.8-um CMOS filter capable of providing 55 dB worst-case image rejection at speeds higher than 140 MHz with a supply voltage of 3 Volts. The 41,848-transistor chip was fabricated via the MOSIS service.

MPA14-3 -- Validation of an Accurate and Simple Delay Model and its Application to Voltage Scaling

Njoelstad, Tormod and Aas, Einar Johan, *Norwegian University of Science and Technology (NTNU)*

A simple, yet accurate, delay estimation model for submicron CMOS is validated by simulation and measurements on several test chips. The validity of the model is demonstrated for simple gates and full adders composed by various circuit techniques, and for complete digital filter designs. The delay model's application to voltage scaling is discussed, in relation to the architecture driven voltage scaling principle. However, sensitivity analysis of the delay model, simulation and test chip measurements indicate that worst case conditions for the process and battery cell voltage may limit the supply voltage reduction for practical reasons. The validated delay model may be used as a delay calculator, and as a mean to trade area against power consumption. Eventually, we suggest a simple, yet efficient, way to explore the initial design space for voltage scaled and multiple-Vdd designs, by combining the delay model and a standard gate level simulator.

MPA14-4 -- A Compact 31-Input Programmable Majority Gate Based on Capacitive Threshold Logic

Leblebici, Yusuf; Gurkaynak, Frank Kagan and Mlynek, Daniel, *Swiss Federal Institute of Technology*

An improved, modular realization of the Capacitive Threshold Logic (CTL) gates is presented which offers significant advantages in terms of silicon area and speed in certain applications. The general architecture and building blocks of the new modular CTL gates is introduced and the operation of the circuit is discussed. The main advantages of the CTL design concept include a very large fan-in capability, compact design, small logic depth and compatibility with conventional CMOS gates. These advantages are illustrated by the design of a 31-input Majority Gate. The CTL realization of the Majority Gate is almost three times faster than a Full Custom standart CMOS Realization and occupies approximately one third of the area which results in a performance increase of nearly an order of magnitude.

MPA14-5 -- A Scalable Shared Buffer ATM Switch Embedded SPRAMS

Jeong, Gab Joong, Shim, Jae Wook, and Lee, Moon Key, *Yonsei University* and Ahn, Seung Han, *Hyundai Electronics Industries Co., Ltd.*

This paper describes the architecture of a scalable shared buffer ATM switch and VLSI implementation. It provides scalability in port size and buffer size. The prototype chip has been designed for 4 x 4 ATM switch which has a shared buffer for 128 ATM cells. It is integrated in 0.6um twin well, double-metal, and single-poly CMOS technology. Operating frequency is 80MHz. Core size is 11mm x 10mm. It supports 622Mbps per port.

MPA14-6 -- Optimum Design for a Two-Stage CMOS I/O Protection Circuit

Li, Tong; Bendix, P., *LSI Logic*; Suh, D.; Huh, Y.J.; and Rosenbaum, E., *Universtiy of Illinois at Urbana-Champaign*; Kapoor, A., *LSI Logic*; Kang, S.M., *University of Illinois at Urbana-Champaign*

In industry, the design of CMOS ESD (electrostatic discharge) protection devices and circuits has been approached empirically. In this work, we propose an optimization methodology for a typical two-stage CMOS I/O protection circuit based on simulation. We have identified two kinds of design, namely resistor-limited and NMOS-limited, and demonstrated that the isolation resistor design is the key to the circuit's protection level and performance.

MPA14-7 -- Low-Swing Charge Recycle Bus Drivers

Karlsson, Magnus; Vesterbacka, Mark; and Wanhammar, Lars, *Linkoping University*

In this paper two robust bus drivers combining low-swing and semi-adiabatic charge recycling technique are presented. The drivers uses a novel concept with schmitt-triggers as voltage sensors [1]. Hence, voltage references are not required. The drivers reduces the power consumption with 55 and 72 percent, respectively.

MPA14-8 -- A Pipelined Architecture of Fast Modular Multiplication For RSA Cryptography

Sheu, Jia-Lin; Shieh, Ming-Der; Wu, Chien-Hsing; and Sheu, Ming-Hwa, *National Yunlin University of Science & Technology*

In this paper, a fast algorithm with its corresponding VLSI architecture is proposed to speed up the modular multiplication with a large modulus. By partitioning the operand (multiplier) into several equal-sized segments, and performing the multiplication and residue calculation of each segment in a pipelined fashion, a performance improvement can be achieved by using our algorithm compared with previous work. We also show an efficient procedure to accelerate the residue calculation and use carry-save addition to implement the architecture such that the critical path is independent of the size of the modulus. Therefore, the resulting architecture and implementation are very suitable to be applied to the high-speed RSA cryptosystem and can be easily implemented in VLSI technology.

MPA14-9 -- Design Methodology of Multiple-Valued Logic Voltage-Mode Storage Circuits

Thoidis, I.; Soudris, Dimitrios J.; Karafyllidis, I.; Thanailakis, A., *Democritus University of Thrace*; and Stouraitis, T., *University of Patras*

A novel methodology designing for Multiple-Valued Logic voltage-mode storage circuits is introduced. Using the proposed inverter-based unit, uni-signal controlled pass gates and True Single-Phase Clocked Logic-based output units, efficient r-ary (where r is the radix) dynamic and pseudo-static latches can be designed. They exhibit regular, modular, and iterative structure, which means that the for Multiple-Valued Logic circuits are VLSI implementable. Also, these circuits use two kinds of MOS transistors, i.e., enhancement and depletion mode. Since we use only clock signal, additional contribution to low power dissipation of the derived circuits is been made. Comparisons with existing circuits prove substantial improvements in terms of speed, power consumption, and transistor count.

MPA14-10 -- Current Sensing Differential Logic (CSDL) for Low-Power and High-Speed Systems

Park, Joonbae; Lee, Jeongho; and Kim, Wonchan, *Seoul National University*

A new low-power high-speed glitch-free logic concept, Current Sensing Differential Logic(CSDL), will be presented. This concept is developed for complex integrated systems of prime importance where the reliability in operation and design flexibility. These performance improvements of power and speed is enabled by restricting the internal voltage swings in the logic evaluation tree. Using the CSDL logic, a 64-bit carry look ahead adder is designed in a 0.6um CMOS technology. The results of the post-layout simulation show that it achieves 2.9ns delay with the power consumption of 21mW at 50MHz with clock buffer.

MPA14-11 -- A Divide-by-4 Circuit Implemented in Low Voltage, High Speed Silicon Bipolar Topology

Schuppener, Gerd; Mokhtari, Mehran; and Tenhunen, Hannu, *Royal Institute of Technology*

This paper presents a Divide-by-4 circuit performing in the GHz range at very low supply voltage. Measurements have shown operation from 2.0-V and 2.2-GHz input frequency, down to 1.1-V and 1.2-GHz. The power consumption is approximately 2.5-mW/latch and 0.3-mW/latch, respectively. The circuit has been designed for nominal 1.5-V operation utilizing the bipolar part of Ericsson Component's 0.6 mm BiCMOS technology (EPIC-3B).

MPA14-12 -- Automated Implementation Of RNS-To-Binary Converters

Henkelmann, Heiko, *University of Bremen*, Drolshagen, A., *Siemens AG*; Bagherinia, H.; Ahrens, H.; and Anheier, W., *University of Bremen*

In this paper we will present an implementation of an RNS-to-Binary Converter based on the mixed radix conversion algorithm by using recently proposed new cell-elements. The proposed architecture can be generated automatically for arbitrary sets of moduli and the method is straight forward. This method is very well suited for standard cell implementations resulting in compact layouts.

MPA14-13 -- A Programmable Image Processing Chip

LeRiguer, E. and Woods, R., *The Queen's University of Belfast;* Ridge, D., *Integrated Silicon Systems* and McCanny, J., *The Queen's University of Belfast*

A new high performance, programmable image processing chip targeted at video and HDTV applications is described. This was initially developed for image small object recognition but has much broader functional application including 1D and 2D FIR filtering as well as neural network computation. The core of the circuit is made up of an array of twenty-one multiplication-accumulation cells based on

systolic architecture. Devices can be cascaded to increase the order of the filter both vertically nad horizontally. The chip has been fabricated in a 0.6u, low power CMOS technology and operated on 10 bit input data at over 54 Megasamples per second. The introduction gives some background to the chip design and highlights that there are few other comparable devices. Section 2 gives brief introduction to small object detection. The chip architecture and the chip design will be described in detail in the later sections.

MPA14-14 -- An Implementation Technique of Dynamic CMOS Circuit Applicable to Asynchronous/Synchronous Logic

Yoshizawa, Hiroyasu; Taniguchi, Kenji; and Nakashi, Kenichi, K*yushu University*

An implementation technique of dynamic CMOS circuit is described. Based on the concept to represent the logic equation making use of the dynamic charge, most of asynchronous/synchronous logic can be implemented in dynamic CMOS circuit.In this paper, D-latch, D-Flip/Flop, JK-Flip/Flop and Phase Frequency Detector are shown that they can be implemented with the concept and technique and it is confirmed by SPICE simulation that they have a comparable or much better performance compared with the circuits designed with the transmission gate.

MPA14-15 -- Design Issues In Cross-Coupled Inverter Sense Amplifier

Hajimiri, Ali, *Stanford University*; Heald, Raymond, *SUN Microelectronics*

This paper presents an analytical approach to the design of CMOS cross-coupled inverter sense amplifiers. The effects of the equilibrating transistors and the tail current source on the speed of the sense amplifier are analyzed. An analysis of the offset due to mismatch in various parameters is performed, showing that a complete offset analysis has to account for the cell and bitline structure. A new figure of merit for the offset in the sense amplifier and several new design insights are introduced.

MPA14-16 -- A Novel Low-Power Building Block CMOS Cell for Adders

Shams, Ahmed M. and Bayoumi, Magdy A., *University of Southwestern Louisiana*

A new low-power, high-speed CMOS 1-bit full adder cell is presented. It is based on recent designs of XOR and XNOR gates, pass-transistors, and it has 16 transistors. This cell has been compared to two widely used efficient adder cells; the transmission function full adder cell (16 transistors), and the low-power adder cell (14 transistors). The new cell has no short circuit power and lower dynamic power, because of less number and magnitude of circuit capacitances. It consumes up to 21% less power than the other two cells, while it is 12% to 20% faster .A comparative analysis (using Magic and Hspice) for 8-bit ripple-carry and carry-select adders shows that the adders based on the new cell can save up to 29% of power consumption.

MPA14-17 -- Modified Half Rail Differential Logic for Reduced Internal Logic Swing

Won, Jae-Hee and Choi, Kiyoung, S*eoul National University*

A modified version of half rail differential logic (HRDL) for reduced internal logic swing is proposed in this paper. The reduced internal voltage swing contributes to lower power consumption when the logic tree implements complex Boolean function. To illustrate the efficiency of the modified logic in power consumption, SPICE simulation results of various logic tree heights for XOR are shown.

MPA14-18 -- A Reconfigurable Integrated Circuit for High Performance Computer Arithmetic

Miller, Neil Linton and Quigley, Steven Francis *University of Birmingham*

In this paper, we present the design of a novel Field Programmable Gate Array (FPGA) which contains the necessary logic elements to support high performance computer arithmetic. The FPGA contains a routing framework and logic cell structure that is suitable for implementing digital systems for computer arithmetic, image processing, digital signal processing and similar computationally intensive applications. The proposed architecture is flexible, reconfigurable and will support operands of various sizes for fixed point parallel and serial binary computations.

MPA14-19 -- Data-driven Self-Timed Differential Cascode Voltage Switch Logic

Mathew, Sanu and Sridhar, Ramalingam, S*tate University of New York at Buffalo*

A new form of DCVS logic, that is self-timed in nature and reduces the overhead of the hand-shaking circuitry has been developed. In comparison with conventional self-timed DCVS, the new data-driven self-timed DCVSL [DSDCVSL] has the advantage of reduced area and smaller delays. It retains the benefits of dual-rail logic and self-timing. The key to efficient functioning of the new scheme lies in the way the completion signal is generated from the output data. This scheme is most applicable to practical circuits where the inputs to a stage arrive from several modules. This would require a proper integration of the completion signals generated by each module into a single signal that can be used to control the gate in question. DSDCVSL performs this integration efficiently.

MPA14-20 -- A Novel Asynchronous Control Unit and the Application to a Pipelined Multiplier

Chiang, Jen-Shiun, *Tamkang University* and Liao, Jun-Yao, *Holtek Corporation*

This paper is to discuss the technique for asynchronous circuit design by using a novel asynchronous control unit. We use the very commonly used device, pass-transistor multiplexer, to design and implement the asynchronous control unit. Even though the architecture of the control unit is simple, the efficiency is well. A multiplier with pipelined structure has been designed to verify the usefulness of this

technique. We use TSMC's 0.6um SPDM process to design and implement an 8-b x 8-b pipelined multiplier. The HSPICE simulation shows that the feed through rate of the inputs can be as high as 250MHz.

MPA14-21 -- The Design and Implementation of an Asynchronous Radix-2 Non-Restoring 32-B/32-B Ring Divider

Chiang, Jen-Shiun, *Tamkang University* and Liao, Jun-Yao, *Holtek Corporation*

Division operation is very important in the computer system. Conventionally synchronous techniques are applied to implement the divider. In this paper we will propose a new asynchronous architecture for the divider. In this asynchronous scheme, the architecture is of simplicity and is very easy for the VLSI implementation. By this asynchronous architecture, we use TSMC!|s 0.6um SPDM process to design a 32-b/32-b radix-2 non-restoring divider. The HSPICE simulation shows that this divider can finish a 32-b/32-b division operation in between 3.7ns to 160.2ns

MPA14-22 -- A Novel Digit-Serial Systolic Array For Modular Multiplication

Guo, Jyh-Huei and Wang, Chin-Liang, *National Tsing Hua University*

In this paper, a novel digit-serial systolic modular multiplier is presented. To the authors' knowledge, this is the very first digit-serial systolic array for modular multiplication. The proposed architecture is highly regular and modular and thus well suited to BLSI implementation. The important feature of the proposed architecture is that different throughput performances can be easily achieved simply by varying the digit size. If the digit size is chosen appropriately, the proposed digit-serial architecture can meet the throughput requirement of a certain application with minimum hardware. The developed modular multiplier is useful in constructing a systolic RSA cryptosystem, where modular multiplication is the kernel operation.

MPA14-23 -- Dual Signal Configuration for Low Power Low voltage High Performance Pipeline Multiplier

Wu, Angus and Ng, C.K., *City University of Hong Kong*

A multiplier cell using dual signal configuration has been used for high performance low power low voltage pipeline multiplier. The proposed configuration requires less number of pipelining buffers; hence, achieving higher efficiency in terms of power consumption and silicon area. The multiplier cell is synchronized with the relocated clocked buffers which are operated with a non-overlapping two-phase clock. Simulation results showed that the proposed circuit delivered two times the throughput and half the pipeline latency of implementations with better power consumption.

MPA14-24 -- Circuit Design for Current-Sensing Completion Detection

Lampinen, Harri and Vainio, Olli, *Tampere University of Technology*

Circuit techniques for Current-Sensing Completion Detection (CSCD) are developed and evaluated. CSCD is a mixed analog-digital method for detecting the completion of operations in digital CMOS. The technique is therefore well suited for controlling self-timed asynchronous digital VLSI circuits. Design of an experimental CSCD chip including digital arithmetic is discussed and the performance of the chip is characterized.

MPA15 Analog and Mixed Signal VLSI Design

Chair: Sherif Embabi **Poster Session**

Texas A&M University

2:00 pm – 5:30pm - ***Room: Serra Ballroom Back III***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

MPA15-1 -- Design of a Delta-Sigma Modulated Switching Power Supply

Dunlap, Steven K., and Fiez, Terri, *Washington State University*

An alternative control solution for a switching power supply using a delta-sigma modulator in place of a PWM controller is presented. The delta-sigma modulator controller does not exhibit the spikes in the noise spectrum characteristic of the PWM controller. A multi-bit delta-sigma modulator controller reduces the output noise floor below the conventional PWM controller noise floor. While the PWM is shown to have better power transfer efficiency, possible alternatives are suggested to increase the delta-sigma modulator controller efficiency.

MPA15-2 -- Theory and Implementation of a Gaussian Decay Low-pass Filter

Harris, John G., and Pu, Chiang-Jung, *U. of Florida*

We have developed a method for approximating a Gaussian decay low-pass filter using subthreshold CMOS VLSI circuits. The time constant (or

σ) of the delay is adjustable over several orders of magnitude and the DC gain is guaranteed to be unity. Since the design is compact and straightforward, the proposed circuit can be used as a building block that can replace first-order low-pass filters in many situations. Gaussian decay circuits have applications in temporal preprocessing for neural networks, demodulation in communication, and auditory sound localization. We also believe that the Gaussian decay function may be superior to other time-delay elements in adaptive filter implementations.

MPA15-3 -- Circuit Tolerances and Word Lengths in Overlap Resolution

Saed, Aryan, Jullien, Graham A., Ahamdi, Majid, and Miller, William C., *VLSI Research Group, University of Windsor*

Overlap Resolution signal processing utilizes residue-like arithmetic and opens up a powerful approach to parallel analog computations with digital accuracy. This new redundant representation of signals, with Continuous Valued Digits, carries the accuracy of analog signal processing beyond the accuracy of the analog circuitry itself. The proposed processing methodology can also be applied to a digital system. Presented tolerances for analog digit circuits and the required digit word lengths for digital circuits show the practical feasibility of Overlap Resolution.

MPA15-4 -- A Design-for-Testability Technique for Detecting Delay Faults in Logic Circuits

Raahemifar, Kaamran, and Ahmadi, Majid, *University of Windsor*

This paper provides a simulation-based study of the delay fault testing in logic circuits. It is shown that delay testing is necessary in order to achieve a high defect coverage. By detecting delayed time response in a transistor circuit, three types of faults are detected: 1) faults which cause delayed transitions at the output node due to some open defects, 2) faults which cause an intermediate voltage level at the output node, and 3) most stuck-at faults which halt the circuit at `1' or `0'. An on-line checker is presented which enables the concurrent detection of delay faults. Since one checker is used for each output signal, the area overhead is minimal. This technique does not degrade the speed of the circuit under test (CUT). We show that the test circuit is independent of the size of the CUT. Simulation results show that this technique can be adjusted to fit to any design style.

MPA15-5 -- About the Demodulation of PWM-Signals with Applications to Audio Amplifiers

Bresch, Helmut, Streitenberger, Martin, and Mathis, Wolfgang, *Otto-von-Guericke Universitae t Magdeburg*

In this paper, the reason for the relatively high distortion level of conventional class-D audioamplifiers is discussed. It is pointed out that the classical approach is insufficient for high performance applications. Therefore the importance of the matching between modulation and demodulation is demonstrated by simulation.

MPA15-6 -- BiCMOS Add-Compare-Select Units for Viterbi Decoders

Demosthenous, Andreas, *University College London*

The add-compare-select unit (ACSU) plays a key role in determining the speed and complexity of a Viterbi decoder. The use of analogue circuit techniques results in a faster, more compact ACSU, which requires less power than conventional digital realisations. This paper describes two BiCMOS high-speed current-mode analogue ACSUs for use in general classes of analogue Viterbi decoders. Metric storage and accumulation employs switched-current techniques and hence no physical MOS capacitors are required.

MPA15-7 -- Deterministic Phase Jitter in Multi-Phase CMOS Ring Oscillators due to Transistor Mismatches

Koneru, S., Chen, Y., Geiger, R., and Lee, E. *Iowa State*

A comparison is made of the effects of random parameter variations on the periodic mismatches in three different high-speed ring oscillators generating multi-phase clock signals. These variations in the phase-to-phase periods manifest themselves in the form of jitter which is deterministic in nature. Simulations have also been carried out to demonstrate the improvement in the jitter performance of these oscillators with device scaling.

MPA15-8 -- A Winner-Take-All Network for Large-Scale Analogue Vector Quantisers

Demosthenous, Andreas, *University College London*

A BiCMOS scalable high-speed current-mode asynchronous Winner-Take-All (WTA) circuit is described. The proposed arrangement is well suited to applications requiring large WTA systems where operating speed and resolution are important parameters, for example, vector quantisation. The WTA has improved resolution and operating speed compared to other current-mode WTAs, especially for large M, where M is the number of inputs. The circuit is very economical in terms of power consumption and operates with 2.8V supply rails.

MPA15-9 -- A Simple Low-Voltage All MOS Linear-dB AGC/ Multiplier Circuit

Brannen, Robert A., Elwan, Hassan, and Ismail, Mohammed, *The Ohio State University*

The design of a simple four-quadrant CMOS multiplier/divider circuit is presented. The new circuit comprises of one transresistance (Norton) operational amplifier and MOS transistors operating in the triode region. A linear-dB, digitally controlled AGC circuit is presented as an application. Simulation results are included to support some of the theoretical claims.

MPA15-10 -- Noise Analysis of an Oscillator with an Mth-order Filter and Comparator-type Nonlinearity

Dec, Aleksander M, *Columbia University*

This paper presents noise analysis of a class of oscillators, which can be modeled by a positive feedback system with a Mth-order filter, a comparator-type nonlinearity, and a white noise input. An analytical expression for the output power spectral density is given. For a special case of a 2nd-order bandpass filter, the expression can be simplified and shown to reduce to a well-known result under a high Q-factor assumption. The theoretical results presented here are verified by experiment.

MPA15-11 -- A 4 GHz Differential Transimpedance Amplifier Channel for a Pulsed Time-of-Flight Laser Radar

Pennala, Riku-Matti, *University of Oulu, Electronics Laboratory*

A wideband differential transimpedance amplifier channel was designed for the receiver of a pulsed time-of-flight (TOF) laser radar using a high frequency bipolar analog array. The measured maximum total transimpedance is ~11 kohm, the bandwidth ~2.5 GHz (limited by the buffer amplifier used for test purposes only, corresponding to an internal bandwidth of ~4 GHz) and the input-referred noise current density ~8 pA/sqrt(Hz). The amplifier channel has a current mode gain control cell in front of the transimpedance preamplifier to reduce the dynamic range of the output signal.

MPA15-12 -- Design of Low Jitter PLL for Clock Generator with Supply Noise Insensitive VCO

Lee, Chang-Hyeon, *USC,* and Cornish, Jack, and McClellan, Kelly, *ADM-Tek* and Choma, Jr,John,*USC*

Supply and substrate noise tend to cause the output clock of PLLs to jitter from their ideal timing. The design of a low jitter PLL has become challenging because of the many design trade-offs between noise and bandwidth. In order to achieve a low jitter PLL design, fully differential signal and control paths of the VCO are maintained. Also, a proposed bandgap regulator helps to achieve high common mode rejection of supply and substrate noise. This proposed bandgap reference serves to reduce oscillator supply and temperature sensitivities and to suppress low/high frequency noise by isolation from supply noise. The simulated oscillator supply noise sensitivity is less than 1 percent/V. Oscillator temperature sensitivity is 500ppm/C in the range of 0 to 100 C. Oscillator Frequency range is 25MHz to 400MHz using a MOSIS 0.8um CMOS process. The clock skew is less than 60ps with a peak-to-peak jitter of less than 100ps for a 200MHz PLL clock frequency.

MPA15-13 -- Novel Palmo Techniques for Electronically Programmable Mixed Signal Arrays

Papathanasiou, Konstandinos, and Hamilton, Alister, *University of Edinburgh*

A novel approach to programmable mixed-signal VLSI is presented that uses a pulse width modulated digital signal to encode analogue signal information. Signal communication between programmable analogue (and digital) signal processing cells is performed using this Palmo signal representation. A linear, programmable, voltage mode analogue CMOS Palmo cell is presented. Results from 1st, 2nd and 3rd order analogue Palmo filters, a 24 tap FIR Palmo filter, and a Palmo sigma-delta analogue-to-digital converter are presented.

MPA15-14 -- A Constant Input Transconductance and Rail-to-Rail Input/Output Swing SiC CMOS OPAMP

Chen, Jian-Song, *Purdue University* and Kornegay, Kevin T.,*Cornell University*

A silicon carbide (SiC) CMOS OPAMP with a constant input transconductance and full input/output voltage swing is presented. A novel bias circuit is used to provide the bias current for both N-channel and P-channel differential pairs a function of the input common mode voltage such that the total transconductance is virtually constant over the entire input common mode range. This scheme is also independent of transconductance parameter matching between the NMOS and PMOS transistors, thus resolving the process variation problem associated with new processes, which may be as high as 100% in the current SiC CMOS technology.

MPA15-15 -- CMOS Analog Multipliers Based on a Class-B Squaring Circuit

Gnudi, Antonio, Pellegrini, Aurelio, Baccarani, Giorgio, *DEIS, Universita' di Bologna*

A class of CMOS analog four quadrant multipliers is proposed based on a squaring block operating in class-B. It is demonstrated that this type of circuit offers better performance in terms of input-range and output-efficiency over traditional solutions, and is less sensitive to transistor parameter mismatch. Measured electrical characteristics of an experimental version of the proposed circuit are also presented.

MPA15-16 A Baseband Pulse Shaping Filter for Gaussian Minimum Shift

Keying

Pavan, Shanthi, *Texas Instruments* , and Krishnapura, Nagendra, *Columbia University*, and Mathiazhagan, Chakravarthy *and* Ramamurthi, *Gaussian*

Pulse shaping is used in digital communication systems like DECT, GSM and WLAN to minimize the out of band spectral energy. The baseband rectangular pulse stream is passed through a filter with a Gaussian impulse response before frequency modulating the carrier. Traditionally this is done by storing the values of the pulse shape in a ROM and converting it to an analog waveform with a DAC followed by a smoothing filter. This paper explores a fully analog implementation of an integrated Gaussian pulse shaper, which can result in a reduced power consumption and chip area.

MPA15-17 A 10-bit 220-MSample/s CMOS Sample-and-Hold Circuit

Waltari, Mikko Eljas and Halonen, Kari, *Electronic Circuit Design Laboratory, Helsinki University of Technology*

A fully differential sample-and-hold (S/H) circuit using double-sampling is presented. Compared to a conventional S/H configuration with a similar opamp the double-sampling gives a factor of two increase in the sampling rate while maintaining comparable power consumption. The circuit is designed in 0.5um CMOS technology. Measurements show 10-bit operation upto the Nyquist frequency at the sampling rate of 220 MS/s with 25 mW @ 3 V power dissipation.

MPA15-18 A Novel Technique for Noise Reduction in CMOS Subsamplers

Lindfors, Saska J., Parssinen, Aarno T., Ryynanen, Jussi H., and Halonen, Kari A, *Helsinki University of Technology*

The operation and design aspects of a receiver with a subsampling mixer are discussed at system level. A novel technique that improves the noise performance of CMOS subsamplers is proposed. The sampling frequency with the proposed structure is fundamentally limited by the speed of the clock generator instead of the hold amplifier as is the case in previously reported subsamplers. A 300MHz test sampler which is designed to be integrated together with a 1.8GHz LNA is described.

MPA15-19 A Novel Self-Error Correction Pulse Width Modulator for a Class D Amplifier for Hearing Instruments

Tan, Meng Tong, *Nanyang Technological University*

In this paper, we propose a novel self-error correction Pulse Width Modulator for a Class D amplifier for hearing aid applications. The self-error correction mechanisms based on Master-Slave architecture is realized by simple digital circuits and can be easily fabricated in a low cost digital CMOS process. The circuit consumes 24.6 uA from a 2.5V supply. Measurements on the prototype IC shows that the error at zero-input 50% duty cycle is less than 2% and the total harmonic distortion is 3.3%.

MPA15-20 An Approach to the Design of Low-Voltage SC Filters

Giustolisi, Gianluca, *DEES - Università di Catania*

A new approach to design low-voltage SC filters is presented. It is based on a simple structure of clock booster and on an SC integrator which uses a single-input transconductance amplifier instead of the traditional differential transconductance amplifier. To validate the approach a low-pass 4th-order elliptic filter with a 1.2 um CMOS process and 1.5-V power supply is designed.

MPA15-21 Design of a Micropower Signal Conditioning Circuit for a Piezoresistive Acceleration Sensor

Silveira, Fernando, Baru, Marcelo Daniel, Picun, Gonzalo, and Arnaud, Alfredo, *Instituto de Ingenieria. Electrica.*

The design and test of a micropower signal conditioning circuit for a piezoresistive accelerometer is presented. The circuit is intended for sensing human body motion in rate-adaptive cardiac pacemakers. A strategy is proposed to allow to handle the piezoresistive sensor with the desired level of consumption. Experimental results show the fabricated circuit is able to measure accelerations in the range from 0.04g to 0.34g with a total consumption of less than 3uA with supply voltages down to 2V.

MPA15-22 A BiCMOS Current-Mode Track-and-Hold

Vasseaux, Tony; Loumeau, Patrick;and Oliaei, Omid, *Ecole Nationale Superieure des Telecommunications*

A current-mode BiCMOS Track\&hold circuit suitable for high-speed low-supply voltage applications is presented. The circuit works with a supply voltage of 2.5V and a clock frequency of 50MHz. It is shown that the BiCMOS realization of SI-circuits offers a good trade-off between power consumption and precision for high-speed applications where a high precision is not needed.

MPA15-23 Analog Implementation of Ratio Spectrum Computation

Harris, John G., Harris, John G. and Lim, Shao-Jen, *University of Florida*

A novel transform space called the RATIO SPECTRUM has been developed. The ratio spectrum is formed by plotting the ratio of the power of a low-pass filtered signal to the power of the original unfiltered signal vs. the filter cutoff frequency. The spectrum is necessarily a monotonic function of frequency that is bounded between zero and one. Though we prove that this transform space is mathematically equivalent to the power spectrum of a signal, the ratio spectrum provides a number of computational advantages. One major advantage is that analog hardware

can efficiently compute the ratio spectrum. Measured results from such an analog VLSI implementation are discussed in this paper.

MPA15-24 Analysis and Two Proposed Design Methodologies for Optimizing Power Efficiency of a Class D Amplifier Output Stage

Tan, Meng Tong, *Nanyang Technological University*

In this paper, we analyze the power dissipation mechanisms and derive the overall power efficiency of a Class D output stage realized using the finger and waffle layouts. We propose two design methodologies to determine the aspect ratios of the transistors in the output stage for optimum power efficiency: (i) optimization to a single modulation index point, and (ii) optimization to a range of modulation indices. For the design of an output stage with optimum power efficiency (and small IC area), we recommend the waffle layout realization optimized to a range of modulation indices. The theoretical analysis and derivations are verified on the basis of computer simulations and measurements on fabricated prototype ICs.

TUESDAY MORNING -- JUNE 2, 1998

Plenary Tuesday

8:05am – 8:45am (Serra Grand Ballroom)

Dr. Robert Trew – Department of Defense,
Office of the Director, Defense Research and Engineering
Title:DOD Basic Research in Circuits and Systems

TAA1-Filter Banks and Wavelets

Chair: Yih-Fang Huang
University of Notre Dame

9:00 am – 12:30pm - ***Room: Colton I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA1-1 -- A Filter Bank - Mother Wavelet Relationship in the Context of the Discrete Time Wavelet Transform

Hanna, Magdy Tawfik, *Cairo University* and Mansoori, Sana Ahmed, *University of Bahrain*

The digital filters a[n] and b[n] of the filter bank required for implementing the discrete time wavelet transform DTWT[m,n] of the sampled signal s(kT) are derived. The filter a[n] is proved to be an all-pass filter and the filter b[n] to be a time-reversed and complex conjugated version of the sampled mother wavelet used in the definition of the DTWT.

TAA1-2 -- Design of Signal-Adapted Linear Phase Paraunitary Filter Banks

Takeuchi, Tomoaki; Nagai, Takayuki; and Ikehara, Masaaki, *Keio University*

In this paper, we propose a new design method of signal-adapted filter banks using an adapted cascade lattice structure. If the filter bank which is well adapted to the signal statistics is used in the subband coding system, we can encode the signal more efficiently than the case using non-adapted one. The purpose of this paper is to design the filter bank which has energy imbalance of each subband. We use LMS-based adaptive algorithm to design linear phase paraunitary filter banks (LPPUFB) based on a lattice structure.

TAA1-3 -- Mutual Relations between Arithmetic and Haar Functions

Falkowski, Bogdan J. *Nanyang Technological University*

Mutual relations between Arithmetic and unnormalized Haar functions are stated. The new relations allow to calculate directly Arithmetic spectrum from unnormalized Haar spectrum and vice verse without the necessity of obtaining back the original function. Since both Arithmetic and Haar spectra are used widely in many applications, the presented equations should further enhance the scope of their applications.

TAA1-4 -- A New Approach to the Design of QMF Banks

Kao, Min-Chi and Chen, Sau-Gee, *National Chiao Tung University*

New L2 objective functions for the design of quadrature-mirror-filter (QMF) banks are proposed. They are based on the derivative information of the reconstruction error. Simple and explicit matrix-form expressions for the proposed objective functions are derived. An efficient design

method is proposed by incorporating a separability technique into the derived optimality conditions on prototype filters. The proposed method only needs to solve linear equations iteratively without nonlinear optimization. Design examples demonstrate that good low-delay QMF banks and linear-phase QMF banks can be obtained after a few iterations. Compared to the conventional approach, the new approach leads to QMF banks with larger stopband attenuation and smaller reconstruction errors.

TAA1- 5 -- Rationalizing the Coefficients of Popular Biorthogonal Wavelet Filters

Tay, David Ban Hock, *Nanyang Technological University*

Many wavelet filters found in the literature have irrational coefficients and thus require infinite precision implementation. One of the most popular filter pairs is the '9/7' biorthogonal pair of Cohen, Daubechies and Feauveau which is adopted in the FBI finger-print compression standard. We present here a technique to rationalize the coeffcients of wavelet filters that will preserve biorthogonality and perfect reconstruction. Furthermore, most of the zeros at z = -1 will also be preserved. These zeros are important for achieving regularity. The rationalized coefficients filters have characteristics that are close to the original irrational coefficients filters. Three popular pairs of filters, which includes the '9/7' pair, will be considered.

TAA1- 6 -- Analytical Design for a Family of Cosine Modulated Filter Banks

Siohan, Pierre and Roche, Christian, *CNET/DMR*

A new family of modulated filter banks has been derived. The design is particularly simple since it is mainly based on a closed-form expression. Nearly perfect reconstruction filter banks are obtained as well as guidelines to estimate the filter bank parameters. Furthermore a slight modification of the prototype filter coefficients is sufficient to exactly satisfy the perfect reconstruction constraints.

TAA1-7 -- Results on Optimal Biorthogonal Subband Coders

Vaidyanathan, P.P. and Kirac, Ahmet, *California Institute of Technology*

The optimization of subband coders for specific input statistics has been an interesting problem for quite some time. For orthonormal filter banks with infinite order and uniform decimation, this problem has been completely solved in recent years. For the case of biorthogonal filter banks significant progress has been made recently, though a number is issues still remain to be addressed. In this paper we present several new results for the biorthogonal case. All discussions are for infinite order (ideal) filters.

TAA1-8 -- An Efficient Algorithm To Design Perfect Reconstruction Regular Quadrature Mirror Filters Using Weighted Lp Error Criteria

Goh,Chee Kiang and Lim,Yong Ching, *National University of Singapore*

An efficient iterative algorithm is presented in this paper to design lattice-type perfect reconstruction regular quadrature mirror filters (PR-QMF) by minimizing the p-th power of an appropriate error criteria, where p can be a function of frequency. The filter bank design is approximated as an unconstrained weighted least squares problem with respect to the lattice coefficients. Typically, only a few iterations of our algorithm is needed to obtain an optimal solution in the weighted Lp sense. An estimation of the number of canonic signed digit(CSD) terms needed to quantize the lattice coefficients yielding minimal degradation of the filter's stop band attenuation is also derived. Efficient multiplierless implementation of lattice-type regular PR-QMF banks are easily obtained using this result.

TAA2 – Modeling, Analysis and Design of Switching Mode Converters

Chair: Henry Chung

City University of Hong Kong *Special Session*

Organizer: Adrian Ioinovici
Holon Institute for Technological Education

9:00 am – 12:30pm - ***Room: Colton II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA2-1 -- Design and Analysis of Quasi-Switched-Capacitor Step-Up C/DC Converters

Chung, Henry S H, *City University of Hong Kong*

A new switched-capacitor (SC)-based step-up DC/DC converter is proposed. It has the prominent features of continuous input current waveform and having better regulation capability than the traditional SC converters. The problem of conducted electromagnetic interference (EMI) with the supply network is minimized. Concept of energy transfer is achieved by using dual basic SC step-up converter cells operating in anti-phase. The voltage conversion ratio is controlled by a current control scheme in order to adjust the charging profile of the capacitors. A generalized n-stage converter is presented and is analyzed by a simplified third order state-space equation set. The static and dynamic behaviors and the design constraints of the proposed converter are derived. A prototype of 30W, 5V/12V, 2-stage converter has been built, giving an overall efficiency of 78% with power density of 15W per cubic inch.

TAA2-2 -- High Efficient PWM Zero-Voltage-Transition DC-DC Boost Converter

Berkovici, J. and Ioinovici, A., *Center for Technological Education Holon*

A soft-switching boost converter with duty-cycle control is proposed. Compared to its hard-switching PSM counterpart, the new switch-mode converter contains four additional elements: a resonant inductor, and active switch and two diodes. The parasitic capacitances of the main and auxiliary active switch serve as resonant capacitors. Multi-resonance is created in the circuit, thus allowing for zero-voltage-switching of the active switches and rectifier diode. The commutation of all switches takes place with zero capacitive turn-on losses; consequently, the switching losses are small. The current through the resonant inductor is not allowed to increase over the load current; the resonant stage is delayed until the inductor has been discharged. As a result, the voltage and current stresses on the devices are at the same level as on their counterparts in conventional converters, implying normal-rated switches, and normal conduction losses. The overall efficiency is very high, as proved by the measurements on a prototype realized in the laboratory.

TAA2-3 -- Bidirectional Buck-Boost Converter with Variable Output Voltage

Krishnamachari, Bhaskar, *The Cooper Union* and Czarkowski, Dariusz, *Polytechnic University*

An increasing number of manufacturing processes rely on ultra-high speed and accuracy machines. Piezoceramic actuators are being utilized as parts of such machines. So far, only linear and switched-capacitor powe rsupplies have been used for driving piezoceramic actuators in such applications.This paper proposes a switch-mode power supply to reduce cost and increase system efficiency. In the proposed design, the traditional PWM buck-boost topology is modified to accommodate bidirectional operation, and dynamic compensation is applied between the reference and the output to ensure good frequency response and low steady-state error of the variable output voltage. The converter operation is verified by Saber simulations.

TAA2-4 -- Sliding Mode Control Of a Buck Converter For AC Signal Generation

Biel, Domingo, Fossas, Enric, Guinjoan, Francesc, and Ramos, Rafael, *Universitat Politecnica De Catalunya*

This work is devoted to the design of a sliding feedback control scheme for a Buck converter in AC signal generation task where amplitude, frequency and offset can be externally adjusted. A sliding control law over an autonomous switching surface is proposed . As a result, the control scheme is found to be robust with respect to parameters variations and external disturbances. Simulations validating the design and some considerations on the control law implementation are also presented.

TAA2-5 -- Novel PWM Control Method of Switched Capacitor DC-DC Converter

Suetsugu, Tadashi, *Fukuoka University*

Switched capacitor converter becomes important as an inductor-less power supply circuit. The big input current ripples and small control width are the problems of switched capacitor converter. PWM method of switched capacitor converter was introduced already, but the control width was not big. In conventional method, the output voltage adjusted by the ratio of discharging and charging time value of the condenser. In this proposed method, the output voltage is controlled by regulating overall length of the dead time. The simulation result shows that the control width of output voltage increased about 1.6 times compared with the conventional method.Furthermore, the ripple of input current also decreased.

TAA2-6 -- True-Worst-Case Evaluation in Circuit Tolerance & Sensitivity Analysis using Genetic Algorithms and Affine Mathematics

Egiziano, l., Femia,N, Spagnuolo, G., and Vocca, G.,*University of Salerno DIIIE*

New methods for circuits Tolerance and Sensitivity Analysis (TSA) are presented in this paper. Genetic Algorithms (GA) and Affine Arithmetic (AA) techniques have been adopted to find respectively the inner and the outer solution in True Worst-Case (TWC) problems for circuits where the strong uncertainty of parameters yields large changes of performances. It is shown that GA and AA allow a sharp determination of the TWC in TSA problems, even of great complexity. Some circuit examples are presented to highlight the accuracy and the efficiency of the new methods, whose application is best suited for the CAD of electronic circuits submitted to performances and regulations constraints to be fulfilled in presence of large parameters uncertainties.

TAA2-7 -- Analytical Solution to Harmonic Characteristics of PWM H-Bridge Converters with Dead Time

Wu, CM, Lau, W.H. and Chung, H.,*City University of Hong Kong*

This paper presents an analytical method to calculate the output harmonic characteristics of PWM H-bridge converters with dead time. A three-dimensional (3-D) model derived for generating the pulse-width-modulated (PWM) pulse train is used to consider the effects of dead time. The harmonic characteristics are obtained by applying the double Fourier series to the output PWM waveform. The results obtained by this new technique are verified with simulations using PSpice.

TAA2-8 – General Purpose Sliding-Mode Controller for Bidirectional Switching Converters

Romero, A., Martinez-Salamero, L., and Vaiderrama, H., *Ecola Tecnica Superior d'Enginyeria*; Pallas, O. and Alarcon., E., *Ecola Tecnica Superior*

d'Enginyerias de Telecomunicacio

A standardized sliding-mode controller for bidirectional switching converters is described. The proposed circuit is suitable for large signal applications and can be used in a large class of dc-to-dc switching converters. As a result, robustness and fast dynamic response against supply, load and parameter variations is obtained. The controller implementation has been performed by means of standard operatoinal amplifiers (OA's) and it has been tested experimentially in elementary and complex switching power converters. An integrated realization of the controller has been simulated at transistor level by means of HSPICE exhibiting similar characteristics to those presented by the OA's-based implementation.

TAA2-9 -- A 1,5kW Two Transistors Forward Converter Using A Non-Dissipative Snubber

Treviso, C.H.G., Pereira, A.A., Farias, V.J., Vieira Jr., J.B. and de Freitas,L.C.,*Universidade Federal de Uberlandia*

This paper will present a 1,5 kW operation with 90% efficiency at full load of a Two Transistors Forward Converter with non-dissipative snubbers. The proposed approach allows building a converter with high frequency operation. A detailed analysis of the operation will be presented. The output voltage is controlled by PWM with a constant frequency. The complete operating principles, theoretical analysis, relevant equations, simulation and experimental results will be presented in this paper.

TAA3-Neural Networks I: Algorithms and Computation

Chair: Robert Newcomb
University of Maryland

9:00 am – 12:30pm - ***Room: Colton III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA3-1 -- On-Line Tracking Abilities of Neural Networks with Graded Responses

Kuh, Anthony, *University of Hawaii*

This paper analyzes the tracking performance of neural networks with graded analog responses when the weights of a target network change slowly with time. We first study the performance of a tracker consisting of a single neuron and then discuss a two-layer network (soft committee machine). The target weights changes depend on the drift rate. The tracker weights follow the LMS algorithm. With a properly chosen step size the tracker network can track the target network with mean squared error depending directly on the drift rate.

TAA3-2 -- A New Class of Apex-Like PCA Algorithms

Fiori, Simone; Uncini, Aurclio; and Piazza, Francesco, *University of Ancona*

One of the most commonly known algorithms to perform neural Principal Component Analysis of real-valued random signals is the Kung-Diamantaras' Adaptive Principal component EXtractor (APEX) for a laterally-connected neural architecture. In this paper we present a new approach to obtain an APEX-like PCA procedure as a special case of a more general class of learning rules, by means of an optimization theory specialized for the laterally-connected topology. Through simulations we show the new algorithms can be faster than the original one.

TAA3-3 -- MultiResolution Neural Networks for Recursive Signal Decomposition

Kan, Kai-chiu and Wong, Kwok-wo, *the City University of Hong Kong*

This paper proposes a novel algorithm for the synthesis of MultiResolution Neural Networks that possesses self-construction capability. It is referred as the Recursive Variance Suppression Growth method. An explicit link between the network coefficients and the Wavelet Transforms is found. By the proposed algorithm, the network is allowed to start with null hidden-layer neuron. As training progresses, the network grows autonomous to tackle the problem being studied. Simulations on a number of natural voice signals and a synthesized piecewise function show that clear and optimal local representation is obtained in spatial-frequency spectrum. This indicates that the proposed approach is superior to the traditional signal decomposition techniques, especially for time-varying signal analysis.

TAA3-4 -- Characteristics of Gradient Descent Learning with Neuronal Gain Control

Ho, Murphy, *City University of Hong Kong* and Kurokawa, Hiroaki, *Keio University*

Human brain shows the capability of adjusting the gain of neurons at the sensory periphery. In this paper, we investigate the properties of backpropagation learning algorithm with adaptive neuronal gain, and compare its performance with the conventional one, and with the one combining dynamic learning rate optimization. Simulation results have shown that the algorithm can achieve the goal of fast convergence, and can alleviate the problem of local minima with a moderate increment of computation and storage burden.

TAA3-5 -- Training of a Class of Recurrent Neural Networks

Shaaban, Khaled M., Assiut University

This paper presents design and analysis of a modified version of the Hopfield network which is called a Cascade Recurrent Network (CRN). This network has a single or multilayer feedforward (FF) structure with synchronous input-output feedback. System dynamics are determined by the characteristics of this FF structure. First, a formal definition of the mapping generalization is provided. Using this definition, and the classical definition of stability, the mapping-stability relation is developed in the form of a correspondence between CRN stability properties and FF mapping characteristics. On the basis of this stability-mapping relation, a new synthesis technique is developed.

TAA3- 6 -- Dynamical Systems Learning by a Circuit Theoretic Approach

Campolucci, Paolo; Uncin, Aurclio; and Piazza, Francesco, *University of Ancona*

In this paper, we derive a new general method for both on-line and off-line backward gradient computation of a system output, or cost function, with respect to system parameters, using a circuit theoretic approach. The system can be any causal, in general non-linear and time-variant, dynamic system represented by a Signal Flow Graph, in particular any feed forward, time delay or recurrent neural network. The gradient is obtained in a straightforward way by the analysis of two numerical circuits, the original one and its adjoint (obtained from the first by simple transformations) without the complex chain rule expansions of derivatives usually employed.

TAA3-8 -- Training RBF Networks with the Kalman Filter

Ciocoiu, Iulian B., Technical University of Iasi

We propose the use of Kalman filter as an alternative to the classical LMS algorithm for training Radial Basis Function (RBF) networks. A state-space formulation for the problem is given and the corresponding equations of the resulting training algorithm are obtained. Simulation results for an example of chaotic time series prediction are presented.

TAA4 – Speech and Video Processing
Co-Chair: Chung-Yu Wu
National Chiao Tung University
Co-Chair: Thanos Stouraitis
University of Patras, Greece

9:00 am – 12:30pm - ***Room: Ferrante I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA4-1 -- Efficient Coding of Linear Predictive Coefficients for Wideband Speech

Magrath, A.J and Sandler, Mark B., *King's College London*

This paper considers the coding of the linear predictive (LP) filter coeffcients for applications where the highest quality natural-sounding speech reproduction is required. Bandwidths as high as 16 kHz and linear prediction orders of 38 are considered. To deal with the increase in model order, a method is proposed to code the trajectory of the line-spectral pair (LSP) representation of the LP coeffcients. To improve the performance of the system, a hybrid scheme if proposed which utilizes a combination of intra-frame LSP coding and trajectory-nased coding. This scheme exploits the reduced sensitivity of the human auditory system to distortion at higher frequencies.

TAA4-2 -- Regressive Linear Prediction with Triplets - An Effective All-Pole Modeling Technique for Speech Processing

Varho, Susanna and Alku, Paavo, *University of Turku*

This paper presents a new linear predictive method for speech processing, Regressive Linear Prediction with Triplets (RLPT). The RLPT-algorithm yields from p normal equations an all-pole filter of order 2p+1 (i.e., an all-pole filter of order 2p+1 is defined from p numerical values). In comparison to conventional linear prediction of order p RLPT takes into account 2p+1 preceding samples of x(n) in the computation of the linear prediction. Consequently, the obtained all-pole filter is able to model the spectrum of voiced speech more accurately than conventional linear prediction, especially with very small p-values. The experiments show that the RLPT-method is effective in finding one or two lowest resonances in voiced speech spectra when p equals 1 or 2.

TAA4-3 -- A Novel Algorithm to Estimate the Line Spectral Frequencies from LPC Coefficients

Nakhai, Mohammad Reza and Marvasti, Farokh Alim, *King's College, University of London.*

A new method to estimate the line spectral frequencies (LSF's) with any desired accuracy is described. LSF's are estimated by locating the zeros of two polynomials derived from LPC inverse filter polynomial on the unit circle in z-plane. The computational load increases as the required accuracy increases. An important feature of algorithm is the ability of compromising the required accuracy and computational load. The method can also be applied to convert the higher order LPC coefficients to associated LSF's. The algorithm does not require a very high precision

arithmetic and can be implemented using fixed-point digital signal processors.

TAA4-4 -- Wideband Speech Recovery From Bandlimited Speech In Telephone Communications

Yasukawa, Hiroshi, *Aichi Prefectural University*

This paper describes methods that can enhance the quality of speech signals that are severely band limited during regular telephone speech transmission. We have already proposed a spectrum widening method that utilizes aliasing in sampling rate conversion and digital filtering for spectrum shaping. This paper discusses the method using linear prediction. Speech components of the outbands of the received signal are basically generated by LPC (linear predictive coding) synthesis by analysis. Furthermore, we discuss a new spectrum widening method using a multilayer backpropagation neural network. It is shown that the proposed method has a good performance of recovering the wideband speech.

TAA4-5 -- An Efficient Method for the Removal of Impulse Noise from Speech and Audio Signals

Chandra, Charu; Moore, Michael S., and Mitra, Sanjit K., *University of California, Santa Barbara*

A computationally efficient algorithm is proposed to remove noise impulses from speech and audio signals while retaining its features and tonal quality. The proposed method is based on the SD-ROM (Signal Dependent Rank Order Mean) algorithm. This technique has successfully been used to remove impulse noise from images. It has the advantage of being relatively fast, simple and robust. The algorithm estimates the likelihood the sample under inspection is corrupt relative to the neighboring samples and replaces a sample detected as corrupted by a value based on the neighboring samples. This algorithm also has the advantage of being `configurable' to the type of noise impulses in the sample, as the thresholds used to detect noise impulses can be varied to suit the signal.

TAA4-6 -- Finite Wordlength Effects Analysis and Wordlength Optimization of Dolby Digital Audio Decoder

Lee, Seokjun and Sung, Wonyong, *Seoul National University*

The finite wordlength effects of a Dolby digital audio decoder are studied using both analytical and simulation-based methods for the wordlength optimization. The wordlength optimization was conducted to minimize the hardware cost while keeping the quantization noise below the human perceptual masking curve. In order to derive an accurate fixed-point error expression using the analytical approach, two kinds of errors, the signal and the coefficient quantizations, are considered separately. In the simulation-based method, 24 sine-wave streams in the center of human ear's 24 critical bands are used, and the frequency regions which are the most critical for fixed-point optimization are determined considering the masking curve. The optimized data-path saves about 14% of the chip area, and 20% of the ROM size when compared with a general purpose DSP data path.

TAA4-7 -- The NLMS Algorithm Using a Quasi-Orthonormal Initialization Scheme for Acoustic Cancellation

Chen, Heng-Chou and Chen, Oscal T.-C., *National Chung Cheng University*

In acoustic echo cancellation, we propose the normalized least-mean-square (NLMS) algorithm with a quasi-orthonormal initialization scheme to overcome slow convergence due to the correlated speech signals. The quasi-orthonormal initialization scheme is realized by a set of the causal sinc vectors which are the low-pass filtered impulse signals at different time-scaled positions. Hence, the loudspeaker-room-microphone (LRM) system can be modeled by these causal sinc vectors. The NLMS algorithm after our initialization processing can efficiently predict the outputs of the LRM system according to the inputs. In case of the outputs of the LRM system corrupted by additive white noises with a variance of 0.0001, the proposed initialization scheme can improve echo return loss enhancement (ERLE) of 50 dB. The computer simulation results demonstrate that finite impulse response (FIR) structure of the NLMS algorithm using the proposed initialization scheme employs fast convergence and low computational complexity.

TAA4-8 -- Motion Estimation Using An Efficient Four-Step Search Method

Chen, Oscal T.-C., *National Chung Cheng University*

Motion estimation using an efficient four-step search method has been developed. It consists of initial-point determination and low-complexity four-step search. For each block, we determine an initial point from the stationary point and motion point with the same displacement of its neighboring block according to their block-matching performances. Based on this initial point, low-complexity four-step search with half-way stop technique is performed to achieve the motion vector. The total number of searching points is varied from 13 to 20. Simulation results show that our method yields a very competitive performance in terms of computational complexity and picture quality as compared to the three-step search, new three-step search, and four-step search methods.

TAA5 – Communicating with Chaos I

Chair: Michael Peter Kennedy

University College, Dublin **Special Session**

Organizers: Michael Peter Kennedy
University College, Dublin
Geza Kolumban
Technical University of Budapest
Sponsor: Technical Committee on Nonlinear Circuits and Systems

9:00 am – 12:30pm - ***Room: Ferrante III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA5-1 -- Recent Advances in Communicating with Chaos

Kennedy, Michael Peter, *University College Dublin;* Kolumban, Geza, Kis, Gabor and Jako, Zoltan, *Technical University of Budapest*

The past few years have witnessed rapid growth in the field of mobile and indoor radio applications. Chaotic communications schemes are potentially suitable for these applications, offering simpler and cheaper solutions that currently available Spread Spectrum (SS) techniques. This paper presents an overview of the most promising chaotic communications schemes which have been developed recently and proposes some multilevel extensions of these methods to increase the data rate.

TAA5-2 -- Statistical Analysis of Chaotic Communication Schemes

Abel, Andreas, Gotz, Marco and Schwarz, Wolfgang, *TU Dresden*

On the base of the estimator variance analysis we present a classification for a number digital chaos communication schemes and conventional spread spectrum techniques, which allows the qualitative comparison of the behaviour of the systems under the presence of additive white Gaussian noise on the channel. The classification results in a ranking and shows that the conventional stored-reference technique outperforms all analyzed chaotic schemes, which reach at most the characteristics of transmitted-reference techniques.

TAA5-3 -- The Performance of Chaos Shift Keying: Synchronization Versus Symbolic Backtracking

Schweizer, Jorg, *Swiss Federal Institute of Technology*

Since Chaos Shift Keying (CSK) has been proposed by H.Dedieu et. al. [Chaos Shift Keying: Modulation and Demodulation of a chaotic carrier using self-synchronizing Chua's circuits, IEEE Trans. Circuits Syst., CAS-40(10):634, October 1993] there has been a number of papers published, dealing with different variations of CSK. However, there is also a deficiency of work devoted to determine the performance of such systems,mainly due to a difficult parameterization. We suggest in this paper to use discrete-time piecewise linear chaotic systems for performance comparisons of CSK. Synchronization of chaotic systems with an in average diverging vector field is in general more sensitive to noise than with a passive system, possessing a converging vector field. We propose therefore a CSK implementation that we term ``symbolic backtracking''. Symbolic backtracking is an algorithm that uses ideas of symbolic dynamics to estimate the initial condition of a finite-length, noise perturbed chaotic trajectory. By ``tracking'' the signal backwards in time the vector field along the trajectory becomes convergent and we expect therefore better performance measures than for a ``forward-oriented'' synchronization technique. We compare finally the performance of CSK with conventional error feedback synchronization against CSK using symbolic backtracking.

Schweizer Joerg *Circuits and Systems Group, Swiss Federal Institute of Technology*

TAA5-4 -- Integrated Circuit Blocks for a DCSK Chaos Radio

Delgado-Restituto, Manuel and Rodriguez-Vazquez, Angel, *Instituto de Microelectronica de Sevilla;* and Porra, Veikko, *Helsinki University of Technology*

A proposal for an integrated digital communication system using a DCSK chaotic modulation scheme is presented. It is a point-to-point wireless system capable of supporting half-duplex real-time voice and low data rate communication (following ISDN standards) in a noisy indoor environment. Design strategies for the integrated realization of the most relevant building blocks of the chaotic modem are also included.

TAA5-5 -- FM-DCSK: A Novel Method for Chaotic Communications

Kolumban, G., *Technical University of Budapest*; Kennedy, M.P., *University College of Dublin*; Kis, G, and Jako, Z., *Technical University of Budapest*

Inbinary Differential Chaos Shift Keying (DCSK), each information bit is mapped to the correlation between two pieces of a chaotic waveform. The receiver determines the correlation (which is proportional to the energy per bit) in order to demodulate the received signal. Since a chaotic signal is not periodic, the energy per bit is not constant and can only be estimated, even in the noise-free case. This estimation has a non-zero variance that limits the attainable data rate. This problem can be avoided if the energy per bit is kept constant. In this paper, the DCSK technique is combined with frequency modulation in order to achieve two properties: the excellent noise performance of DCSK is maintained; in addition, the energy per bit is kept constant in order not to limit the data rate. A low-pass equivalent model that significantly speeds up the simulation of an FM-DCSK system is also developed. Finally the noise performance of the proposed FM-DCSK system is given.

TAA5-6 -- High Rate Data Communication using Dynamical Chaos

Dmitriev, Alexander Sergeevich; Yemetz, Sergei; and Starkov, Sergei Olegovich, *IRE RAS*

Communication scheme for high rate information transmission using dynamical chaos is suggested. A novel method is presented for encoding and trans-mitting digital data by means of chaotic dynamical systems. This scheme is demonstrated to transmit more than one bit per chaotic sample. The main features and the robustness of the suggested method with respect to the channel noise are discussed.

TAA5-8 -- Sequence Synchronization in Chaos-Based DS-CDMA Systems

Mazzini, Gianluca, *CSITE – CNR*; Rovatti, Riccardo and Setti, Gianluca, *University of Bologna*

The aim of this contribution is to consider a further step in the study of the impact of chaos-based techniques on classical DS-CDMA systems. The problem addressed here is the sequence phase acquisition and tracking which is needed to synchronize the spreading and despreading sequences of each link. An acquisition mechanism is proposed and analyzed in depth to identify parameters allowing the study of its performance when classical and chaos-based sequences are employed for spreading. Numerical results show that the adoption of chaos-based techniques may lead to improvement in link startup delay and expected service availability.

TAA5-9 -- Implementing RF Broadband Chaotic Oscillators: Design Issues and Results

Silva, Christopher Patrick and Young, Albert M., *The Aerospace Corporation*

The recent discovery of chaotic synchronization has spawned a flurry of activity in applying chaos to communications. These efforts have sought to explore the potential capabilities/benefits of the three basic elements in a chaos-based communications system: the chaotic carrier, the synchronization process, and the carrier modulation. The heart of these systems is the chaos generator that must be configured to produce the generalized carrier. Several generator implementations have been developed, including low-frequency analog and digital circuits, and high-frequency analog phase-locked loops and negative-resistance-based oscillators. This paper surveys efforts to push chaos generation from baseband to a wideband high-frequency regime, forming the basis for a broadband microwave chaos-based communications system. Several key circuit implementation issues involving this frequency migration will be identified and discussed. Accomplishment highlights will be presented, including the invention of a novel wideband high-frequency chaotic oscillator design approach.

TAA7 –Nonlinear Networks and Systems

Chair: K.S. Chao

Texas Tech University

9:00 am – 12:30pm - ***Room: Bonzai I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA7-1 -- A Simple Bracketing Algorithm for Determining Transition Time Instants in PWL Circuits

Pastore, Stefano, *Universita di Trieste*; and Premoli, Amedeo, *Politecnico di Milano*

The paper presents a new simple and robust algorithm for determining the transition time instants between adjacent linear regions in the time domain analysis of piecewise-linear (PWL) circuits. The algorithm is based on appropriate PWL functions, versus time, bounding lower and upper the voltages and currents controlling the PWL elements.

TAA7-2 -- Global Asymptotic Stability of a Class of Nonlinear Dynamical Systems

Xiong, Kaiqi, *North Carolina State University*

In this paper we systematically study the global asymptotic stability of a class of nonlinear dynamical systems based on the Liapunov function method. We obtain necessary and sufficient conditions (NASCs) for the existence of a Liapunov function of Lurie type with negative semi-definite derivative. We improve the Moore-Anderson theorem and the Popov frequency criterion in this field. An illustrative example is provided.

TAA7-3 -- A Discrete–Time Approach to the Steady State Analysis of Distributed Nonlinear Autonomous Circuits

Bonet-Dalmau, Jordi; Palà, Pere; and Miró, Joan Maria, *UPC-Department of Signal Theory and Communications*

We present a new method for the steady state analysis of autonomous circuits with transmission lines and generic nonlinear elements. With the temporal discretization of the equations that describe the circuit, we obtain a nonlinear algebraic formulation where the unknowns to be determined are the samples of the variables directly in the steady state, along with the oscillation period, the main unknown in autonomous circuits. An efficient scheme to build the Jacobian matrix with exact partial derivatives with respect to the oscillation period and with respect to the samples of the unknowns is described. To illustrate the proposed technique, the time–delayed Chua's circuit is analized in its periodic zones.

TAA7-4 -- Bifurcation of Switched Nonlinear Dynamical Systems

Ueta, Tetsushi; Kousaka, Takuji; and Kawakami,Hiroshi, *Tokushima University*

Differential equations including discontinuous characteristics have been studied for the last two decades. These systems are easily realized by electric circuits with switches; conparator using an OP amp, relayswitches, thyristors and so on. Although the systems might be includeing chaotic dynamics, they are focused on their behavior around equilibrium points and stabilizing control for steady states in engineering fields. A circuit with hysteresis (discontinuous) characteristic as a chaotic oscillator is proposed by Saito[1].. He analyzed its properties by using rigorous solution and return map. The analysis can be possible because the model is piecewise linear. On the other hand, dynamical systems described by Co-class differential equations (i.e., continuous but non-differentiable can behave also chaotically. Chua's circuit[2], Inaba's circuit[3] are typical systems of this class of dynamical system. These are also piecewise linear, so they can be analyzed rigorously. In view point of numerical analysis, non-smooth characteristics of above two kinds of dynamical systems, especially latter case, are approximated by

smooth functions for convenience of calculation. This method is practical and useful, however, obtained solutions and bifurcation structure are slightly different form one of the original model. In this paper we consider these non-smooth characteristics as piecewise-defined functions split by their break points. The Poincarè sections are naturally defined at the break points and the Poincarè mapping is constructed as a composite map of local mappings. The parameter values of local bifurcations are calculated by Newton's method using these mappings. Additionally the global bifurcations are also obtained by similar method. We propose a standard method to calculate bifurcation parameter values of these systems, and show an illustrated example. This method gives a systematic approach to qualitative analysis of switched dynamical systems.

TAA7-5 -- -Chaos Generators with Piecewise Linear Trajectories

Tsubone, Tsdashi Sailo, T.; and Schwarz, W., *Hosei University*

Novel autonomous chaos generators with piecewise linear trajectories are proposed. We consider three and four dimensional versions of the chaos generators and analyze the dynamics using mapping procedures. An simple implementation examples are also provided and its chaotic behavior is demonstrated.

TAA7-6 -- Spatiotemporal Pattern from a Simple Hysteresis Network

Jinno, Kenya; and Tanaka, Mamoru, *Sophia University*

In this paper, we analyze output sequences which generate from a simple hysteresis network (ab. SHN). The SHN is a dynamical system with a continuous time, discrete space, continuous state and discrete output. The SHN is a quite simple, but it exhibits various kinds attractors: stable equilibria, periodic and non-periodic attractors. We focus on the output sequence corresponding to the attractor of non-periodic state. The results indicate that the output sequence of chaotic attractors can be classified into temporal pattern and spatiotemporal pattern.

TAA7-7 -- Analysis of a Simple Hysteresis Neural Network and Its Application

Nakaguchi, Toshiya; Jinno, Kenya; and Tanaka, Mamoru, *Sophia University*

This paper describes analysis of synchronization phenomena from a simple hysteresis network which consists of three cells. We focus on the relation between time constants and bifurcations. And we consider about applying into quantizer. After making an experiment of quantizer with simulation, we realize the quantizer and obtain desirable result.

TAA7-8 -- Effects of the Deviation of Element Values in a Ring of Three and Four Coupled Van der Pol Oscillators

Oakawara, Tsoyoshi and Endo, Tetsuro, *Meiji University*

This paper investigates the effect of element value deviation on the degenerate mode in rings of three and four coupled van der Pol oscillators. By using the averaging method, we elucidate that the element value deviation has different effects on the rings of three and four coupled oscillators. Namely, for the ring of three coupled oscillators, two single modes, which bifurcate from the two-fold degenerate mode in the symmetric system can be synchronized when they are close, but they lose synchronization and a quasi-periodic oscillation appears when they are separated to some extent. In contrast, for the ring of four coupled oscillators, the two single modes cannot be synchronized even if they are close, but in some rare cases they can be synchronized when they are separated to some extent. We confirm these results of the averaging method by both computer simulation and experiments.

TAA8 – Amplifiers I

Chair: Edward Lee

Iowa State University

9:00 am – 12:30pm - ***Room: Bonzai II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA8-2 -- A 3.3-V CMOS Wideband Exponential Control Variable-Gain-Amplifier

Huang, Po-Chiun, Chiou, Li-Yu, and Wang and Chorng-Kuang, *National Central University*

A CMOS cascadable variable gain amplifier (VGA) with exponential gain control characteristic is presented. The pseudo-exponential gain control function is realized by a source-coupled pair with diode-connected loads. It is suitable for low supply and high speed applications. Using 0.5mm CMOS technology, experimental results show the bandwidth of the proposed amplifier is larger than 150MHz with a gain control range of 15dB. The power consumption is 12.5mW from a 3.3-V power supply.

TAA8-3 -- Systematic Generation Of Transconductance Based Variable Gain Amplifier Topologies

Klumperink, Eric A. M., *MESA Research Institute, University of Twente*

A systematic method for the generation of variable gain amplifier topologies is proposed. The generation is based on voltage controlled current sources (VCCSs) modelling saturated MOS transistors, resistors or combinations of these elements. It is shown that many alternative circuit topologies can be generated, that would not easily have been found in an intuitive way. Simulation results shown that significant differences in performance occur, with various mixes of specific strong and weak points. The set of alternative topologies can be used as a circuit topology database for analogue CAD systems.

TAA8-4 -- Low Noise Current-Mode CMOS Transimpedance Amplifier for Giga-bit Optical Communication

Park ,Sung Min, *Imperial College of Science, Technology and Medicine*

A novel current-mode CMOS transimpedance amplifier is described. The design uses a common-gate regulated cascode configuration providing low input impedance and low input current noise. HSPICE simulations using a 0.6um CMOS process give 3.5GHz bandwidth, 61dB transimpedance gain, 4.2pA/sqrtHz equivalent input noise current spectral density, and 135mW power consumption. Measured results of a previous test chip are also presented.

TAA8-5 -- A CMOS Automatic Gain Control for Hearing Aid Devices

Silva-Martinez, Jose, Salcedo-Suner, and Jorge, *Instituto Nacional de Astrofisica Optica y Electronica*

In this paper a CMOS Automatic Gain Control (AGC) for Hearing aid devices is proposed. Montecarlo analyses have shown total harmonic distortion below 0.5% and 0.6% for uncompressed and hard compressed operations, respectively. Dynamic Range is 69 dB while the THD is around 0.5%. Power consumption for the complete AGC is 54 micro watts for maximum compression operation. Attack and release times are below than 5ms. The AGC is Operated with +1.5, and -1.5 supply voltages.

TAA8-7 -- An Amplifier Design Methodology Derived from a MOSFET Current-Based Model

Schneider, Márcio Cherem, Pinto, Rodrigo and Luiz de Oliveira, *Universidade Federal de Santa Catarina*

This paper presents a design methodology for MOS amplifiers based on a universal model of the MOSFET, valid from weak to strong inversion. A set of very simple expressions allows quick design by hand as well as an evaluation of the design in terms of power consumption and silicon real estate. The design and integration of a common-source amplifier illustrate the appropriateness of the proposed methodology.

TAA8-8 -- A 3-V CMOS Optical Preamplifier with DC Photocurrent Rejection

Phang, Khoman, Johns, David A., *University of Toronto*

This paper describes a CMOS optical preamplifier suitable for free-space, infrared wireless communications. The design is differential for improved power supply noise rejection, and an active cancellation scheme is used for eliminating DC photocurrents that are generated by ambient light. Making use of a 0.35-um CMOS process, the preamplifier provides a transimpedance gain of 20 kohms over a bandwidth from 1 MHz to 100 MHz and achieves 60 dB attenuation at dc.

TAA9 – Logdomain Filters

Chair: Alison Payne

Imperial College, London, England

9:00 am – 12:30pm - ***Room: Bonzai III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA9-1 -- A Fully-Programmable Analog Log-Domain Filter Circuit

Roberts, Gordon W., and Hematy, Arman, *MACS Laboratory, McGill University*

This paper will describe the design of a general purpose continuous-time IF analog filter that utilizes log-domain integrator circuits. The coefficients of the filter are digitally programmable and externally controlled using a serial input data stream. Both the poles and the zeros of the filter are adjustable, allowing arbitrary filter function implementation. The filter has been fabricated in a 0.8 micron BiCMOS technology and it is capable of 2.5 volt operation. The experimental results are included.

TAA9-2 -- Fully Differential Class-AB Log-Domain Integrators

Wu, J. and El-Masry, Ezz I., *DalTech, Dalhousie University*

A new fully balanced log-domain integrator structure is proposed. The use of the differential structures can reduce the distortion and improve the dynamic range of the circuits. Two balanced versions: the complementary transistor pair (CTP) and the all-npn transistors, are introduced. The circuits were verified by the simulations of a 5th-order Chebyshev low-pass filter.

TAA9-3 -- Multiple Feedback Log-Domain Filters

Drakakis, E.M.; Payne, A.J., and Toumazou, C., *Imperial College*

In this paper the design of a Multiple Feedback FLF log-domain filter is presented by means of the Bernoulli Cell-based "Log-domain State Space" differential equations. Confirming HSPICE simulation results are presented.

TAA9-4 -- Synthesis of Distortion Compensated Log-Domain Filters using State Space Techniques

Frey, Douglas, *Lehigh University*

A new state space method is proposed for the synthesis of "Quasi-Log domain" filters where the parasitic emitter resistance of transistors is built into the equation formulation. The explicit exponential maps for Log Domain filters are replaced with implicit exponential maps yielding modified nodal equations for active filters. Circuit realization is discussed and some example circuit topologies are proposed. Finally, the extension to general higher order filters is suggested.

TAA9-5 -- An Auto-Biased 0.5um CMOS Transconductor for Very High Frequency Applications

Garrido, Nuno Miguel de, Franca, and Jose Epifaneo da, *Instituto Superior Tecnico*

This paper describes a CMOS transconductance cell for the implementation of very high frequency current-mode gm-C filters. It features simple pseudo-differential circuitry employing small device size transistors and yielding a power dissipation of less than 1 mW/pole at nominal 3.0V supply voltage. Self-biased common-mode voltage designed to minimize mismatch errors, improves noise and stability behavior. Short channel effects are analyzed and simulation results are presented.

TAA9-6 -- Noise in High-Order Log-Domain Filters

Punzenberger, Manfred, *Swiss Federal Institute of Technology,(EPFL)* and Enz, Christian C., *Rockwell Semiconductor Systems,*

The noise performance of high-order log-domain filters in the presence of an input signal is investigated. It is shown, that class AB log-domain filters behave like distributed companding systems. The results are extended to a 3rd-order Chebyshev filter and are in good agreement with measurements of a BiCMOS implementation.

TAA9-7 -- Low-Voltage Current-Mode CMOS IC Continuous-Time Filters with Orthogonal W0-Q Tuning

Shana'a, Osama, *Stanford University* and Schaumann, Rolf, *Portland State University*

The design of fully differential high-frequency continuous-time current-mode filters in digital CMOS technology is presented. A universal biquad is constructed from two basic building blocks, lossless and lossy differential current-mode integrators. The circuits are very simple, can readily be integrated, are suitable for high-frequency applications, and can operate with a power supply as low as 3V. Pole frequency wo and quality factor Q are turned orthogonally by means of a translinear circuit. The orthogonal wo-Q tuning method permits the design of digitally programmable analog filters where all programming activities take place in the DC bias circuitry, with no switches and their unavoidable parasitics in the signal path. The design is illustrated on a 100MHz fifth-order cascade lowpass filter, simulated for a standard 0.6m digital CMOS process. With 3V supply voltage and 1200mA bias current, power dissipation equals 4.2mW per biquad. Total harmonic distortion (THD) was simulated to be -84dB. Implementations in bipolar, CMOS or biCMOS are possible; no special technology is required.

TAA9-8 -- Analysis of Noise in Translinear Filters

Mulder, Jan, *Delft University of Technology*

To describe the effects of noise in translinear filters, large-signal equations have to be used, due to the internal non-linearities and the non-stationary nature of the noise sources .In this paper, a noise analysis method is proposed, which takes into account the non-linear and non-stationary aspects. As an example, the signal x noise intermodulation is calculated for a class A and a class AB operated log-domain filter.

TAA10 – Oversampled Data Converters

Chair: Raymond Chik
Quantum Corporation

9:00 am – 12:30pm - ***Room: San Carlos I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA10-1 -- Micro-Power 10-Bit Sigma-Delta A/D-Converter

Rapakko, Harri Antero, *Nokia Mobile Phones*

A 10-bit sigma-delta A/D-converter was designed to study the aplicability of the new type of SC-integrator circuit. The new topology utilizes the constant gate-source voltage of a source follower instead of utilizing the virtual short circuit between the input nodes of the operational

amplifier. The main benefit of the of integrator circuit is the considerably decreased current consumption and smaller silicon area. The measurement results showed that the main limiting factor of the topology was the low DC-gain, which lead to improper noise shaping. The other properties of the charge transfer based on constant gate-source voltage were promising, especially when used in battery-operated low-power electronics.

TAA10-2 -- An Area-Efficient Sigma-Delta DAC with a Current-Mode Semidigital IFIR Reconstruction Filter

Kim, Jae-Wan, *Korea University,* Min, and Byung-Moo, *LG semicon Co., Ltd. ,and* Yoo, Jang-Sik, and Kim, Soo-Won, *Korea University*

This paper introduces an area-efficient sigma-delta DAC structure with an interpolated noise shaper and a semidigital interpolated finite impulse response (IFIR) reconstruction filter. Applying the IFIR approach to the design of reconstruction filter, we reduce the number of required reconstruction filter coefficients almost by factor of two. Thus, the realized sigma-delta DAC exhibits robust reconstruction filter response with reduction of active area

TAA10-3 -- A 1V Second-Order Sigma-Delta Modulator

Salama, C. Andre T and Ma, Stanley Jeh-Chun, *MOSAID Technologies Inc./University of Toronto*

This paper presents a low-power, low-voltage second-order sigma-delta modulator operating from a 1 V power supply. The modulator is implemented in a 0.5 um CMOS process with a 0.32 V threshold voltage transistors. The modulator achieves a dynamic range of 14 bits for an input bandwidth of 7 kHz while dissipating only 425 uW.

TAA10-4 -- Mismatch-Shaping DAC for Lowpass and Bandpass Multi-Bit Delta-Sigma Modulators

Shui, Tao, *Oregon State University,* and Schreier, Richard, *Analog Devices Inc. and* Hudson, Forrest, *Veris Industries, Inc.*

Techniques similar to delta-sigma modulation can be used to spectrally shape the static mismatch errors of multi-bit delta-sigma converters. Algorithms to shape the mismatch-error for lowpass and bandpass applications are covered. Both simulation and test results show that the signal-to-noise and distortion-ratio (SNDR) of a delta-simga DAC is improved when mismatch-shaping is used.

TAA10-5 -- Mismatch Cancellation for Double-Sampling Sigma-Delta Modulators

Yu, Li, *Carleton University*

The performance of double-sampling sigma-delta A/Ds can suffer due to capacitor mismatch as well as uneven clock phases. Improving the resulting SNR is essential. This paper presents a method that uses DSP techniques to filter out the mismatch. Simulation results of applying an adaptive LMS filter to a fourth-order double-sampling bandpass sigma delta modulator are presented that show an improvement in SNR of more than 30 dB.

TAA10-6 -- Power Optimization of Delta-Sigma Analog-to-Digital Converters based on Slewing and Partial Settling Considerations

Fiez, Terri, and Naiknaware, Ravindranath, *Washington State University*

A technique to obtain low power delta-sigma ADC designs under slewing and partial settling behavior of the integrators is described.delta-sigma ADCs do not require complete settling of the integrators to the overall converter accuracy due to their oversampling and noise-shaping characteristics. When the slewing and incomplete settling behavior of the modulator are explored properly, it is possible to obtain power optimal designs. Accurate estimates are obtained under non-ideal conditions such as finite switch resistances in the sampling and the feedback paths. It is also shown that the noise reduction strategies such as correlated double sampling (CDS) significantly affect the powerrequirements.

TAA10-7 -- Nonuniform-to-Uniform Decimation for Delta-Sigma Frequency-to-Digital Conversion.

Galton, Ian,, *University of California, San Diego*

Recently, a delta-sigma frequency-to-digital converter (FDC) capable of 14-bit audio bandwidth data conversion at a 10MHz intermediate frequency (IF) was presented. The nonuniform-to-uniform decimation filter, a key component of this FDC, corrects for the nonuniform sampling inherent to the FDC and performs decimation filtering. This paper contains a detailed description of the nonuniform-to-uniform decimation filter and measured performance results for the entire FDC.

TAA10-8 -- A Single-path Multi-bit DAC for LP Delta-Sigma A/D Converters

Louis, Loai, and Roberts, Gordon W., *MACS Laboratory, McGill University*

A multi-bit DAC based on encoding DC levels in bitstreams is introduced. The DAC converts the multi-bit digital value into bitstreams which are then filtered by an analog filter to extract the DC levels encoded therein. With this approach, one analog path is used for all levels, thus reducing mismatch effects. A prototype IC has been fabricated in a 0.8 um BiCMOS process incorporating the DAC in a 2nd-order Switched-Capacitor (SC) LP Delta-Sigma modulator.

TAA11 – Digital Signal Processing for Hearing Aids Special Session

Chair: Neeraj Magotra

University of New Mexico

9:00 am – 12:30pm - ***Room: San Carlos II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA11-1 -- Recruitment Compensation as a Hearing Aid Signal Processing Strategy

Allen, Jont B, *AT&T Labs -- Research*

Although Fowler is commonly given credit for discovering recruitment (Fowler36), Steinberg and Gardner at Bell Labs (Steinberg37b) were the first to understand its true significance.Today recruitment is poorly understood, and is generally misdefined as the abnormally rapid growth of loudness. It is not well known that loudness in sones does not grow more rapidly in the recruiting ear; rather it is the intensity of an equally loud tone (i.e., the loudness--level in phons) that grows more rapidly. Regardless of the definition, recruitment is the most basic manifestation of sensory--neural hearing loss. Recruitment is due to the loss of outer hair cell (OHC) function. The sound--detecting inner hair cells (IHC) within the cochlea have a limited dynamic range of less than 60 dB. The OHCs nonlinearly compress the dynamic range of the signal excitation to the IHC, extending its dynamic range. Thus the normal function of OHCs plays a critical role in loudness and speech coding. Distortion product otoacoustic emissions (OAE) are an objective measure of OHC nonlinear compression, while loudness growth is a subjective measure. This report discusses the application of multiband compression (MBC) to the compensation of loudness recruitment. This technology was ``reinvented'' at Bell Labs between 1983 and 1987 and is now sold by the ReSound Corporation. Our basic strategy with multiband compression is to restore the normal dynamic range which is lost due to OHC misfunction. I describe why MBC works and what the hair cells do. In the oral presentation I shall describe how the OHCs might do act as compressors (see my web site). Finally I review the history of the MBC hearing--aid development at Bell Labs.

TAA11-2 -- A Flexible Filterbank Structure for Extensive Signal Manipulations in Digital Hearing Aids

Brennan, Robert and Schneider, Todd, *dspFactory*

Filterbanks for digital hearing aids must use significantly different criteria than those designed for coding applications. For digital hearing aids, the filterbank channel gains must be adjustable over a large dynamic range to compensate for the hearing loss. This adjustability isolates the alias cancellation properties of critically sampled filterbanks designed for coding. This paper describes a filterbank designed exclusively for hearing aid applications. Consideration will be given to the extremely limited memory, low delay and low power requirements that must be met in a typical hearing aid application.

TAA11-3 -- Multiband Compression Hearing Aids: Developing a Performance Metric

Schmidt, Jon C., *Starkey Laboratories* and Rutledge, Janet C., *University of Maryland at Baltimore*

When attempting to compare different compression algorithms used in multiband compression hearing aids, or different parametersettings of a given compression algorithm, there is a need to compare equivalent amounts of compression. Since there are several parameters that influence the actual amount of compression that occurs, it is desirable to know which set of parameters will create the least perceptual difference from the original signal for a given amount of compression. Unfortunately, there is not a well defined approach for determining the amount of compression that has been imparted to a signal. Two degree of compression metrics are proposed that can be used to determine the amount of compression by direct analysis of the audio signal before and after compression. These metrics give excellent results in predicting the ratings of subject-based testing on the audio quality of several different audio segments across several parameter variations.

TAA11-4 -- Multichannel Compression in the Normal Ear and as a Signal Processing Algorithm for the Hearing Impaired

Yund, E. William, *Veterans Affairs Northern California Health Care System*

The nature of sensorineural hearing loss (SNHL) indicates that full-range multichannel compression (FRMCC) signal processing will help the hearing-impaired. Our recent studies of speech perception in hearing impaired subjects support the value of FRMCC with at least 8 channels, especially when the signal-to-noise ratio (S/N) is low. Results from other laboratories, however, have been less favorable. The particular acoustic conditions used in these experiments, plus the restricted time subjects have to acclimatize to each signal processing algorithm, seem to account for the differences among studies, but field testing of FRMCC is needed. Developments in digital signal processing (DSP) have made it possible to plan extensive field tests of binaural 8-channel FRMCC. Hearing-aid users will be able to evaluate the FRMCC in all the acoustic environments they normally encounter, both during and after full acclimatization to the signal processing.

TAA11-5 -- Multichannel Adaptive Noise Reduction in Digital Hearing Aids

Magotra, N., Kasthuri, P., Yang, Y., and Whitman, R.,*University of New Mexico; and* Livingston, F., *Texas Instruments Incorporated*

We have developed a digital binaural hearing aid using Texas Instrument's floating point TMS320C3X digital signal processing (DSP) chip. The device is referred to as the Digital Programmable Hearing Aid (DIPHA). It has the capability of being programmed to perform a variety of speech processing tasks and is in essence a digital hearing lens. It permits matching the processing strategy to an individuals specific hearing loss. This paper deals with the adaptive noise reduction algorithm employed by DIPHA. Typically the audiologist/therapist selects a number of bandpass filters to design (in effect) a custom binaural equalizer for the hearing impaired subject and cascades the noise reduction algorithm with the equalizer. This paper explores the concept of performing the adaptive noise reduction in individual bands of the equalizer, a multichannel adaptive noise reduction strategy for the hearing impaired.

TAA11-7 -- Signal Processing Techniques for a DSP Hearing Aid

Edwards., Brent W., *ReSound Corporation*

The recent development of commercial hearing aids with digital signal processing (DSP) capabilities opens the door for an explosive growth in hearing aid sophistication. Current limitations on signal processing design due to hearing aid constraints, andthe specialized needs of listeners with hearing loss, result in certain design specifications that any DSP hearing aid must meet. This paper will review the latest state-of-the-art with respect to current DSP hearing aids on the market, with an emphasis on the ReSound programmable DSP hearing aid, developed in a collaboration with GN Danavox and AudioLogic, Inc. Multiband compression, single-microphone processing, multi-microphone processing, and feedback reduction will be discussed.

TAA12 – Analog Circuit Design
Chair: Chorng-Kuang Wang
National Central University, Taiwan

9:00 am – 12:30pm - ***Room: San Carlos III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA12-1 -- Statistical Behavioral Modeling of Integrated Circuits

Swidzinski, Jan Feliks; Styblinski, M.A.; and Xu, Gonggui, *Texas A&M University*

A full statistical model for the behavioral parameters of an analog cell is presented. Behavioral parameter variations with respect to manufacturing process disturbances are approximated utilizing multivariate modeling techniques which allow the means, standard deviations, parameter correlations and the actual distributions to be reproduced with reasonable accuracy. The modeling procedure is demonstrated in statistical behavioral modeling of a MOSFET-C notch filter at the cell level and a phase-locked loop (PLL) tunable filter at the system level. The accuracy of the results obtained utilizing the characterized behavioral MOSFET-C filter and the PLL models, relative to the circuit-level simulation is considered.

TAA12-2 -- Robust Recursive Inverse Approximation and its Application to Parameter Extraction of Behavioral Models

Xu, Gonggui and Styblinski, M.A., *Texas A&M University*

An algorithm, Robust Recursive Inverse Approximation (RRIA), for parameter extraction in the statistical IC modeling is presented. RRIA gives very accurate modeling parameter formulas based on observation data after the behavioral model is set up. It can extract the parameters simultaneously for multiple circuits which have same structure but with different parameter values. RRIA combines Newton-Raphson, least-squares and Singular Value Decomposition techniques. The theory of this algorithm is presented in details. Its efficiency for different modeling levels is verified by two examples: the MOSFET device and the bandpass filter.

TAA12-3 -- Study of Optimal Importance Sampling in Monte Carlo Estimation of Average Quality Index

Keramat, Mansour and Kielbasa, Richard, *SUPELEC*

In this contribution, the optimal Importance Sampling, which is a variance reduction technique in Monte Carlo estimation, is theoretically studied in the case of electronic circuits. To the best of our knowledge, this problem has previously not been studied in electronic circuits. In this study, the theoretical basis of the optimal importance sampling is developed in the case where no approximate model of the circuit responses is given. Simulation results show good agreement with the theoretical basis.

TAA12-4 -- Worst-Case Analysis of Linear Analog Circuits using Sensitivity Bands

Tian, Michael W. and Shi, Richard, *University of Iowa*

A novel approach for frequency-domain worst-case analysis is proposed in this paper. It is based on the fact that if a circuit response is monotonic with respectto the changes in a circuit parameter value, then the extreme values of the response occur at theextreme values of that parameter. The monotonicity is identified by the sensitivity band computation over the parameter space, and is used to reduce the number of uncertain parameters in circuit simulation. These ideas are implemented in a prototype circuit

TAA12-5 -- Fast Time Domain Noise Simulation of Sigma-Delta Converters and Periodically Switched Linear Circuits

Dong, Yikui and Opal, Ajoy, *University of Waterloo*

This paper presents fast time domain methods for computer simulation of electrical noise and sampling-clock jitter in sigma-delta data converters and in general periodically switched linear networks, such as, switched capacitor filters at circuit macro-model level. The proposed methods have been implemented in a computer program SDNoise. In this paper, examples of thermal noise simulation in a switched capacitor filter and in a sigma-delta A/D converter are given. Examples of sampling-clock jitter simulation are also given for the sigma-delta A/D converter in the case when it is used to conver tbaseband signal, and in the case when it is used as IF front-end to convert IF signal by sub-sampling technique. Simulation time in the order of minutes is shown for 74k clock-cycle data of the sigma-delta A/D converter when thermal noise and clock jitter are present.

TAA12-6 -- Efficient Utilization of On-chip Inductors in Silicon RF IC Design Using a Novel CAD Tool; The LNA Paradigm

Papananos, Yannis, and Koutsoyannopoulos, Yorgos, *National Technical University of Athens*

A CAD tool for modeling planar and multi-layer polygonal integrated inductors on silicon substrates has been developed. The tool can be used in the efficient design of RF ICs containing on-chip inductors. The accuracy and reliability of the software is established through measurement results. The CAD tool is then used in the extraction of design guidelines for the development of inductor structures suitable for a given application. This procedure is demonstrated with the design of an LNA.

TAA12-7 -- OPTOMEGA: An Environment for Analog Circuit Optimization

Keramat, Mansour, and Kielbasa, Richard, *Ecole Superieure d'Electricite (SUPELEC)*

The development of OPTOMEGA, an environment of analog circuit optimization, is presented. OPTOMEGA communicates with the electric circuit cimulater OMEGA and the Matlab engine by the Interprocess Communications (IPC) techniques. We have used the Matlab engine as a subenvironment for pre-developing functions and methods and a post-processing tool in order to map the circuit responses on desirables performances. OPTOMEGA consists of the nomial circuit optimization by globaloptimization algorithms and the parametric yield or Average Quality Index (AQI) optimization. The tool includes effcient Monte Carlo analysis algorithms which ensure an extensive verification and characterization of the design. Two circuit optimization examples are given.

TAA12-8 -- AC Constraint Transformation for Top-Down Analog Design

Arsintescu, Bogdan G., *Delft University of Technology*; Charbon, Edoardo; Malavasi, Enrico; and Kao, William, *Cadence Design Systems*

In mixed designs, analog blocks are often the most difficult parts to realize, due to the large number of high-level constraints and the importance of second order effects. In this paper a method is proposed to automatically transform AC constraints from higher to lower levels of hierarchy within a top-down design methodology. The transformation consists of finding a linear approximation for the analytic expression of the transfer function for flat and hierarchical designs. A state-of-the-art filter design example illustrates the capabilities of the method.

TAA13-Adaptive Signal Processing I — Poster Session

Chair: Paulo S. Diniz
Federal University of Rio De Janiero

9:00 am – 12:30pm - ***Room: Serra Ballroom Back I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA13-1 -- A New Delayless Subband Adaptive Filter Structure

Diniz, Paulo Sergio Ramirez, *Federal University of Rio de Janeiro*

Adaptive subband techniques have been developed to reduce complexity and slow convergence problems of the traditional fullband high-order adaptive filters. In this paper, we present a new delayless maximally decimated structure where the optimal subband filters are related to the wideband system in a closed form, and it is based on the analysis carried out for the delayless scheme previously proposed by the authors. The proposed structure makes use of a special DFT analysis filter bank where the polyphase components of the prototype filter represent fractional delays so that there is no need for adaptive cross-filters and the unknown system can modeled perfectly in a closed loop scheme. Some computer simulations are presented in order to verify the good features of the proposed structure.

TAA13-2 -- On the Design of the Target-Signal Filter in Adaptive Beamforming

Joho, Marcel, *and* Moschytz, George S., *Swiss Federal Institut of Technology*

This paper deals with the improvement jammer suppression for adaptive broadband beamforming. The analysis is carried out with a 2 microphone Griffiths-Jim Beamformer and one jammer signal. By examination of the derived optimal filter, a design strategy for the constant target signal filter in the main channel of the beamformer is given. This leads to a substantial reduction in the required filter

length of the adaptive filter while maintaining the same jammer suppression. Furthermore, a faster rate of convergence can be achieved, as there are less filter coefficients that have to be adapted. Finally, it is shown that the design strategy also applies if more than two microphones are used.

TAA13-3 -- A New Modified Variable Step Size for the LMS Algorithm

Okello, James, Itoh, Yoshio, Fukui, Yutaka, and Nakanishi, Isao,*Tottori University* and Kobayashi, Masaki; *Ibaraki University*

Adaptive FIR digital filters which uses the LMS algorithm have found application in quite a wide area of digital signal processing due to their simplicity. In all these areas of application, the measurement of good performance has always been a faster convergence compounded with minimum misadjustment. However, with the LMS algorithm, a higher convergence speed is always complemented by a higher misadjustment. In trying to overcome this trade off, different kinds of variable step size algorithms and the modified variable step size algorithm have been proposed. Unfortunately these algorithms are affected by colored disturbance signal. In this paper we propose a new modified variable step size algorithm, which is independent of both white and colored disturbance noise.

TAA13-4 -- Adaptive Prediction of Sample Values for Digital Transducers

Hölling, Matthias; Thaler, Markus; and Troster, Gerhard; *SwissFederal Institute of Technology*

In the following, we present a method to scale down the dynamic requirements of current sensors by adaptive prediction of the next sample value. Using magnetic field sensors to measure current, a compensation field can easily be generated by a feedback current. If the compensation field corresponds in magnitude to the field generated by the primary current, the current sensor only needs to be linear within a much smaller range, thus, the resolution can be increased. The prediction is done by applying LMS-adaptation rules on previous samples of the resulting magnetic field. This works well for wide sense stationary and periodic signals, and it requires a certain learning time until accurate results are achieved. Applications for this system can be found in the field of current measuring devices for low voltage networks in power distribution systems.

TAA13-5 -- "A DSP-Based Modular Architecture for Noise Cancellation and Speech Recognition"

Gómez, Pedro; Álvarez, Agustín; Martínez, Rafael; Rodellar Victoria; Pérez-Castellanos; and Nieto, Victor; *DATSI, Universidad Politecnica de Madrid*

Through the present paper the architecture of a low-cost Hardware Building Block (HBB) Board for Signal Processing is presented. An overview of the algorithms to be supported by the HBB is followed by a brief presentation of the low-cost hardware platform based on the TMS320C31, interfacing with a host computer through a PCI bus. A description of the modular solutions based on this board for Isolated Word Speech Recognition in Noisy Environments is also given. Measurements of the real-time performance of the card and several Noise-Canceling experiments are also shown. Applications of the proposed architecture may be found in the field of Speech Training, Language Acquisition, Phonetics, and others related.

TAA13-6 -- An Efficient Approach to Noise Suppression in Adaptive Filtering Subject to Output Envelope Constraints

Zheng, Wei Xing, *University of Western Sydney*,

Median smoothing is incorporated into the recently developed adaptive envelope-constrained filtering algorithms with a view to suppressing the effect of impulsive noise at the input channel. It is demonstrated that the proposed adaptive filtering algorithms can provide notable improvements in the performance. In particular, the output envelope constraints of primary interest can be more easily satisfied by the filter weight estimate obtained with the median smoothing than with the average smoothing in impulsive noise situations.

TAA13-7 -- A Feedback ANC System Using Adaptive Lattice Filters

Yeung, Tak Keung and Yau, Sze Fong, *The Hong Kong Universityof Science and Technology*,

This paper investigates the feedback active noise control system which consists of three modules: predictor, identifier and equalizer. The predictor is implemented by an adaptive transversal FIR filter. A new adaptive lattice filter is proposed to construct the identifier which is constrainted to be minimum- phase. The reflection coefficients of the identifier are then used to form a lattice IIR filter for equalization with guaranteed stability. Simulation results show that adopting the adaptive lattice filters for identification and equalization achieve excellent performance, and the feedback ANC system is effective for low-frequency noise reduction.

TAA13-8 -- Pipelining of 2-Dimensional Adaptive Filters Based on the LDLMS Algorithm

Kimijima, Tadaaki; Nishikawa, Kiyoshi; and Kiya, Hitoshi, *Tokyo Metropolitan University*

In this paper we propose a new adaptive algorithm for 2-dimensional pipelined adaptive filters and its hardware architecture. The proposed algorithm is based on the LDLMS algorithm, and it can be achieved both of good convergence characteristics and high throughput simultaneously.

TAA13-9 -- Transform-Domain Delayed LMS Algorithm and Architecture

Wu, An-Yeu and Wu, Cheng-Shing, *National Central University*

The least mean square (LMS) algorithm is one of the most widely applied adaptive methods in communications systems due to its simplicity. In applications that require high-speed sampling rate and very long tap FIR filter, the delayed LMS (DLMS) is usually employed. However, the

value of the delay stage (D) will lead to degradation of the convergence speed, which is not acceptable in fast time-varying communication channels. In this paper, we propose a new DLMS algorithm called "Transform-domain DLMS (TD-DLMS)" to overcome the aforementioned speed degradation. It is derived based on the multirate FIR filtering structure, and the operations are performed in the transform domain. By doing so, the delay stage (D) in the DLMS can re reduced to D/M-1+2log2(2M), where M is the decimation factor. As a result, we can reduce the value of D that causes slow convergence rate in the DLMS. Besides, since the adaptive filtering is performed in the transform domain, we can apply the technique of "power normalization" to further improve the convergence rate.

TAA13-10 -- Generalization of Exponentially Weighted RLS Algorithm Based on a State-Space Model

Lee, Yong Hoon; Kim, Beomsup; and Chun, Byungjin, *Korea Advanced Institute of Science and Technology*

We develop a generalized RLS (G-RLS) algorithm described by a state-space model through some modification of the procedure for Kalman filter derivation. It is shown that the G-RLS algorithm reduces to the conventional RLS when the state transition matrix is an identity matrix, and that the G-RLS algorithm without exponential weighting and Kalman filtering become identical when the state model is an unforced dynamical model. The G-RLS algorithm does not require model statistics, and can be implemented once the forgetting factor is chosen. The performances of the G_RLS and Kalman filtering are compared through computer simulation. Specifically, they are applied to the derivation of variable loop gains of a digital phase-locked loop (DPLL). The results indicate that the G-RLS algorithm can act like the Kalman filter if its forgetting factor is properly chosen.

TAA13-11 -- Adaptive Spectral Estimation Based on Exponential Model

Sanubari, Junibakti, and Tokuda, Keiichi, *Satya Wacana University*

In this paper, a new adaptive filter algorithm is proposed. The adaptive filter is based on the exponential (EXP) filter. Since it has been proved that EXP filter has an infinite impulse response, this adaptive filter is appropriate to replace the IIR adaptive filter which is based on irrational form. To speed up the convergence, we use a similar approach as in the RLS method.

TAA13-12 -- LMS/LMF and RLS Volterra System Identification based on Nonlinear Wiener Model

Chang, Shue-Lee, and Ogunfunmi, Tokunbo, *Santa Clara University*

This paper presents the LMS/LMF and RLS adaptive filtering algorithms based on the nonlinear Wiener model for Volterra system identification. This Wiener model contains three sections: a single-input multi-output linear with memory system, a multi-input, multi-output nonlinear no-memory system and a multi-input, single-output amplification and summary system. For Gaussian white input signal, because of the orthogonality of the Q-polynomial, the autocorrelation matrix can be diagonalizable which allows us to apply LMS algorithm without an y difficulty. This result can also be extended easily to LMF algorithm family. If we apply RLS, the faster convergence speed can be expected. In certain circumstances, the nonlinear Wiener model allows us to identify a complicated Volterra system with only very few terms but still keep the linear filtering properties which means that we can achieve good performance without sacrificing the computation complexity.

TAA14- VLSI II — Poster Session

Chair: Sudhakar Muddu

Silicon Graphics

9:00 am – 12:30pm - ***Room: Serra Ballroom Back II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA14-1 -- Synthesis of Critical ASICs with Embedded Fully Concurrent Cault Resilience

Hamilton, Samuel Norman and Orailoglu, Alex, *University of California, San Diego*

As society has become more reliant on electronics, the need for fault tolerant ICs has increased. This has given rise to a large class of ASICs for which erroneous behavior or unexpected downtime can have costly or even life threatening results. We are proposing the first fully automated approach to concurrent fault identification and reconfiguration in ASICs.

TAA14-2 -- A Low-Power GaAs MESFET Dual-Modulus Prescaler

Kanan, Riad; Hochet, B.; Kaess, F.; and Declercq, M., *Swiss Federal Institute of Technology*

A structure for a high speed low-power GaAs dual-modulus frequency divider is presented in this paper. By using a new flip-flop, simulations predict a lower power consumption than previously reported CMOS and GaAs circuits.
The prescaler has been fabricated with a standard 0.6mm MESFET technology verifiying the expected low power dissipation.

TAA14-3 -- A Noise-Based Random Bit Generator IC for Applications in Cryptography

Petrie, Craig Steven, and Connelly, J. Alvin, *Georgia Institute of Technology*

The design of a random bit generator (random number generator) analog IC suitable for integration with VLSI cryptographic systems is presented. Certain applications in cryptography require the production of an unpredictable and unbiased stream of binary data derived from a fundamental noise mechanism. A prototype random bit generator IC was constructed and tested to be functional for bit rates up to 1.4 MHz. The experimental system passes many standard randomness tests even when exposed to non-random influences such as power supply noise and substrate signal coupling. The system occupies a chip area of 1.5 mm^2 in a 2-micron CMOS technology and dissipates 3.9 mW of power.

TAA14-5 -- 44 Gbit/s 4:1 Multiplexer and 50 Gbit/s 2:1 Multiplexer in Pseudomorphic AlGaAs/GaAs-HEMT Technology

Nowotny, Ulrich; Lao, Z.; Thiede, A.; Lienhart, H.; Hornung, J.; Kanfel, G.; Hohler, K.; and Glorer, K., *Fraunhofer-Institut fuer Angewandte Festkoerperphysik*

Using our 0.2µm AlGaAs/GaAs quantum well high electron mobility transistor (HEMT) technology, we have developed time division multiplexer chips. A 2:1 Multiplexer for data rates up to 50 Gbit/s and a 4:1 Multiplexer designed for easy implementation into existing fiber-optical digital transmission systems to speed up their data rates to 40 Gbit/s. Both circuits can be operated on a single power supply in the range of -3 V to -5.5 V. The power dissipation is 2.8 W and 1.7 W respectively at 4.0 V supply voltage.

TAA14-6 -- Floating-Gate CMOS Analog Memory Cell Array

Harrison, Reid R., *California Institute of Technology*; Hasler, Paul, *Georgia Institute of Technology*; and Minch, Bradley A., *Cornell University*

The complexity of analog VLSI systems is often limited by the number of pins on a chip rather than by the die area. Currently, many analog parameters and biases are stored off chip. Moving parameter storage on chip could save pins and allow us to create complex programmable analog systems. In this paper, we present a design for an on-chip non-volatile analog memory cell that can be configured in addressable arrays and programmed easily. We use floating-gate MOS transistors to store charge, and we use the processes of tunneling and hot-electron injection to program values. We achieve greater than 13-bit precision with no crosstalk between memory cells.

TAA14-7 -- The Most Resistive Model For The MOS Resistive Circuit

Osa, Juan I.; Porta, Sonia; and Carlosena, Alfonso, *Universidad Publica de Navarra*

Significant departures between predicted behaviour and actual performance are observed in opamp based structures containing the so called MOS Resistive Circuit. In this contribution we demonstrate that the usual description of this cell by a simple model of two tunable resistors is not adequate enough to properly shape the MRC operation. A more complete, though still simple model is proposed and shown to work through some examples.

TAA14-8 -- Novel Input ESD Protection Circuit With Substrate-Triggering Technique in a 0.25-mm Shallow-Trench-Isolation CMOS Technology

Ker, Ming-Dou; Chen, Tung-Yang, and Wu, Chung-Yu, *National Chiao-Tung University;* Tang, Howard; Su, Kuan-Cheng; and Sun, S.-W., *United Microelectronics Corp.*

A substrate-triggering technique, to increase the ESD robustness and to reduce the trigger voltage of the ESD protection device, is proposed to improved the ESD-protection efficiency of the input ESD protection circuit in deep-submicron CMOS technology. Through suitable substrate-triggering design on the device structure, this proposed input ESD protection circuit can successfully protect the thinner gate oxide (50 A) of the input stage in a 0.25-um CMOS technology and sustain an ESD level above 2000V without extra process modification.

TAA14-9 -- Dynamic-Floating-Gate Design For Output ESD Protection In A 0.35-mm CMOS Cell Library

Ker, Ming-Dou, *Industrial Technology Research, Institute;* Chang, Hun-Hsien; Wang; Chen-Chia; Yeng, Horng-Ru; and Tsao, Y.-F., *Taiwan Semiconductor Manufacturing Company*

A dynamic-floating-gate design is proposed to improve ESD robustness of the driving-current-programmable CMOS output buffers in a 0.35-um CMOS cell library. through suitable design to dynamically float the gates of the output NMOS/PMOS which are originally unused in a 2-mA output buffer, the ND-mode (PS-mode) ESD level of the 2-mA output buffer can be improved from the original 1.5 KV (1.0KV) up to greater that 8KV.

TAA14-10 -- Fully Integrated Readout Channel with Amplitude and Time Measurement for AMS Experiment on ISSA

Baschirotto, Andrea, *University of Pavia/I.N.F.N.*, Boella, G., *I.N.F.N.*, Castello, R., *University of Pavia/I.N.F.N.*; Frattini, G., *University of* Pavia; Pessina, F., *I.N.F.N.*, Rancoita, P.G., *I.N.F.N.*

A readout channel to be used in the A.M.S. (Anti-Matter Spectrometer) to be installed on the International Space Station Alpha (I.S.S.A.) is proposed. The read-out channel perform time and amplitude measurement. The whole readout system has been designed in HF3CMOS, a BiCMOS technology with 1.2µm minimum CMOS channel length. The system operates with a single 4V supply consuming 4.8mW.

TAA14-11 -- Optimum SNS to Binary Conversion Algorithm and FPGA Realization

Pace, P.E., *Naval Postgraduate School;* Styer, D., *University of Cincinnati* and Ringer,W.P., *Naval Postgraduate School*

Folding analog-to-digital converter, fold the input signal symmetrically in order to reduce the number of comparators required to amplitude analyze the signal (preprocessing). The optimum symmetrical number system (OSNS) formulation is a direct consequence of the need to extract the maximum amount of information from a symmetrically folded waveform. OSNS folding converters require the minimum number of comparator circuits for any desired resolution. Although there is a direct correspondence between the OSNS and the residue number system, the

symmetrical residues cannot be converted to a binary value (e.g., using the Chinese Remainder Theorem) in a straightforward manner. This paper presents and efficient algorithm that converts the symmetrical residues within a three moduli (2k + 1, 2k , 2k -1) OSNS to the equivalent binary representation. Also presented is a pipelined field programmable gate array (FPGA) realization of the algorithm.

TAA14-12 -- Switched-Capacitor Interpolator for Direct Digital Frequency Synthesizers

Santos, Paulo Jorge and Franca, José E., *Instituto Superior Técnico Center for MicroSystems*

Direct Digital Frequency Synthesis (DDFS) is an attractive alternative to PLL-based synthesizer architectures, mainly due to a better frequency agility and inferior phase noise. For current technologies such synthesizer architectures tipically operate below 100 MHz due to power dissipation constraints and speed limitations. In this paper we propose an alternative architecture that allows a pratical speed improvement of DDFS circuits. This consists of using a switched-capacitor (SC) interpolator inserted between the digital-to-analog converter (DAC) and the continuous-time output filter and which allows a relaxation of both the filter selectivity requirements as well as the DAC clock frequency. By choosing an optimum ladder-based architecture for the implementation of such interpolator, the opamps can be designed to settle at the lower input frequency, and thus reducing their own speed and power dissipation requirements, while maintaining low amplitude response variability against component errors.

TAA15- CAD I — Poster Session

Chair: Douglas J. Fouts

Naval Postgraduate School

9:00 am – 12:30pm - ***Room: Serra Ballroom Back III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAA15-1 -- Maximally Routable Switch Matrices for FPD Design

Chang, Yao-Wen and Wu, Guang-Min, *National Chiao Tung University*

An FPD switch matrix is said to be maximally routable if it has the maximum routing capacity among all switchmatrices of the same size. In this paper, we present two classes of most economical maximally routable switch matrices.

TAA15-2 -- Fault Emulation with Optimized Assignment of Circuit Nodes to Fault Injectors

Sedaghat-Maman, Reza, *Institute of Microelectronic Systems University of Hanover*

Fault injection into an optimized circuit is made possible with the introduction of additional logic called Fault Injectors, which are controlled by a Fault Activator. In order to attain an optimum utilization of FPGA resources a novel technique is presented for the assignment of nodes and corresponding Fault Injectors in the matrix form of the Fault Activator.

TAA15-3 -- State-space Technique for Minimal Realization of Analogue Circuits and Systems

Kadim, H.J., *University of Hull*; and Arslan, Tughrul, *Cardiff University of Wales*

An analogue circuit's behaviour can be represented by a number of natural modes. To ensure the compliance of the circuit to a prescribed specification, it is important to test the circuit against the performance of its natural modes. Unspecified mode's characteristics, which could be due to disturbances in the form of faults (i.e. hard or soft), can indicate abnormality in circuits specified behaviour. The work presented here is twofold: (i) an investigation of systems dynamics to estimate the reliability of the circuit when operating in the presence of faults; (ii) a proposed method for minimal realization.

TAA15-4 -- Precise-MD: A Software Tool for Resources Constrained Scheduling of Multi-Dimensional Applications

Hua, Jia; Rashid, Obaidur; Passos, Nelson L.; Halverson, Ranette H.; and Simpson, Richard P., *Midwestern State University*

Nested loops, usually found within the multi-dimensional (MD) computation problems, can be modeled as MD data flow graphs (MDFGs). In order to optimize such loops, a scheduling technique able to achieve parallel execution in the loop body is required. This paper presents a software system, Precise-MD, designed to solve such problems. Precise-MD allows the user to input the MD problems represented by MDFGs through a graphical interface and then applies an MD-Scheduling algorithm, OPTIMUS, which is able to obtain the shortest schedule length for a resource constrained system in polynomial time. Experiment results demonstrate the usability and application of this tool.

TAA15-5 -- Redesignability Analysis of Digital VLSI Circuits with Incomplete Implementation Information

Wey, Chin-Long and Khalil, Mohammad Athar, *Michigan State University*

This paper describes a new problem of digital circuit design -- redesign of digital VLSI circuits with incomplete implementation information., and presents a solution -- redesign process. Efficient algorithms are developed to derive the transfer functions of the portion with incomplete implementation information. Thus, the portion can be re-implemented using the derived transfer functions. We do not intend to discover the exact

circuit schematic and components that were present in the circuit originally implemented. Rather, the functions originally intended to be present will be identical. A set of simple rules is proposed in this study to quickly analyze the redesign-ability of a target circuit.

TAA15-6 -- Fuzzy Multiobjective Decision Making On Modeled VLSI Architecture Concepts

Jeschke, Hartwig, *Universitaet Hannover*

This paper discusses a novel approach for the support of decisions on alternative architectural concepts. Multiple objectives for cost and performance are applied. Analytical performance models have been extended by fuzzy arithmetic. Known analytical efficiency measures are generalized by a fuzzy multiobjective decision making approach. The proposed modeling technique has been implemented by a new tool, the VSP Decision Program, which flexibly supports the high-level specification and evaluation using various performance models.

TAA15-7 -- Parallel Coprocessor Architectures for Molecular Dynamics Simulation: A Case Study in Design Space Exploration

Gerber, Martin and Goessi, Thomas, *Swiss Federal Institute of Technology*

The purpose of the paper is to describe a new semi-automated design space exploration method based on genetic programming. A new control/dataflow specification method is proposed as well as appropriate models for hardware parts and algorithms. With this method we are able to test many different hardware architectures and algorithms against cost, speed, computation time and other constraints within very short time. The remaining manual work is to exploit the model parameters of the components of the architecture and the algorithm. In contrast to other approaches our method is suited for embedded and distributed systems. The method, models and application are explained in detail by means of a comprehensive case study.

TAA15-8 -- Dual Edge Operations in Reduced Ordered Binary Decision Diagrams

Miller, D. Michael, *University of Victoria*; Drechsler, Rolf, *Albert-Ludwigs-University*

The use of input and output negation in reducing the size of ROBDDs has been well investigated. Here we consider duality, a fundamental property of Boolean functions, and how it can be used to further reduce ROBDD size. We show how to introduce dual edge markers into a ROBDD package with effectively no storage overhead and a very small increase in per node processing cost. Our experimental results show that dual markers can reduce the size of the ROBDD, sometimes quite substantially, and even in cases where they offer little reduction, can still lead to increased overall processing speed. We consider the variable reordering problem and sifting in particular. We show that dual markers can not be used directly in shifting, but show that there is substantial advantage in applying sifting to an ROBDD with output negations, followed by a second phase where dual markers are used to reduce the size of the ROBDD.

TAA15-9 -- ROBDD as a Recursively Defined Periodic Bit-String

Lee, Seong-Bong; Yeon, Kwang-Il; and Park, In-Hak, *Semiconductor Technology Division, ETRI*

The paper describes bit-string interpretation of ROBDDs. ROBDDs are viewed as recursively defined periodic bit-strings and BDD operations as recursively defined bit-wise operations. Using the periodicity of bit-strings, we prove that the ROBDDs generated by rotating the bit-string of a ROBDD are mutually different. It implies not only the exponential BDD size but also more compact BDD representation. And the interpretation can explain the hidden ideas of variable ordering.

TAA15-10 -- Generation of Quasi-Optimal FBDDs through Paired Haar Spectra

Chang, Chip-Hong, *Nanyang Polytechnic* and Falkowski, Bogdan J., *Nanyang Technological University*

A polynomial Haar expansion for unnormalized Haar transform of incompletely specified Boolean function has been derived. Based on the Haar expansion, the entropy and equivocation in probability theory have been formulated in terms of some subsets of coeffcients from the recently introduced Paired Haar spectrum. A unified and systematic method founded on the concept of entropy has been developed to exploit the don't care sets of incompletely specified Boolean functions for the heuristic minimization of Free Binary Decision Diagrams. The approach is general and can be extended to other combinatorial decision problems.

TAA15-11 -- Calculation of Paired Haar Spectra for Systems of Incompletely Specified Boolean Functions

Falkowski, Bogdan J., *Nanyang Technological University*; and Chang, Chip-Hong, *Nanyang Polytechnic*

A new algorithm is given that converts a reduced representation of Boolean functions in the form of disjoint cubes to unnormalized Paired Haar spectra for systems of incompletely specified Boolean functions. Since the known algorithms that generate unnormalized Haar spectra always start from the truth table of Boolean functions the method presented computes faster with a smaller computer memory. The method is extremely effcient for such Boolean functions that are described by only few disjoint cubes and it allows the calculation of only selected spectral coeffcients, or all the coeffcients can be calculated in parallel.

TAA15-12 -- Pseudo-Symmetric Functional Decision Diagrams

Chrzanowska-Jeske, Malgorzata; Ma, Xiang Ying; and Wang, Wei, *Portland State University*

A new algorithm for generating a regular logic structure, Pseudo-Symmetric Functional Decision Diagrams (PSFDDs), for completely specified

Boolean functions is presented. The diagrams are based on Functional Decision Diagrams (FDDs) and Pseudo-Symmetric Binary Decision Diagrams (PSBDDs). A Davio expansion is used to generate the initial vertex subfunctions which are then modified by a new Join-XOR operation. The operation allows to combine adjacent vertices such that the function is represented as a regular pseudo-symmetric network which can be easily implemented with an array of AND/XOR gates. Due to the regular structure the interconnection length is known from the logic representation so the post-layout delays can be accurately predicted before the layout is completed.

TAA15-13 -- A New Lock based State Coding Methodology for Signal Transition Graphs

Nagalla, Radhakrishna, *University of New South Wales*

In this paper a new approach for enforcing complete state coding (CSC) property in Signal Transition Graph (STG) specifications will be discussed. As a novel contribution we propose a lock based methodology to ascertain whether a given STG has complete state coding property. Unlike most of the existing methods which operate on a state graph, our method operates on the STG. This approach has the advantage of being either easily automated or easier to visually correlate with the STG specifications. Experimental results with a large number of practical asynchronous bench marks are presented.

TAA15-14 -- Multi-input/multi-output Block Diagram Grammar

Adachi, Yoshihiro; Kobayashi, Suguru and Tsuchida, Kensei, *Toyo University*

A multi-input/multi-output block diagram grammar for a block diagram with multiple inputs and/or multiple outputs is formalized in terms of a context-sensitive graph grammar. This grammar is defined by adding to the single-input, single-output block diagram grammar we proposed previously dummy nodes and new productions for dealing with multiple inputs and/or multiple outputs. A parser based on the multi-input/multi-output block diagram grammar is also implemented; it uses a bottom-up parallel algorithm to parse diagrams with multiple inputs and/or multiple outputs. The block diagram grammar defined in this paper makes a fundamental and important formal model for system analysis and design using block diagrams on a computer.

TAA15-15 -- Improved Minimization Methods of Pseudo Kronecker Expressions for Multiple Output Functions

Lindgren, Per, *Lulea University of Technology, Sweden* and Drechsler, Rolf and Becker, Bernd, *Albert-Ludwigs-University*

Pseudo Kronecker Expressions (PSDKROs) are a class of AND/EXOR expressions. For a Boolean function with a given variable order the minimal PSDKRO can be derived efficiently using Decision Diagram (DD) techniques. The quality, i.e., the number of products in the expression, of the result is known to be dependent on the variable ordering. This paper proposes several improvements and enhancements to previous minimization methods. A pruning technique that can be tuned to tradeoff quality for computational resources is presented. By applying dynamic ordering methods, significant improvements to many previously reported results are obtained. Furthermore,a new method for the minimization of multiple output functions is outlined. Experiments on a set of MCNC benchmarks confirm the advantages of the presented algorithms.

TAA15-16 -- Computational Experience with a Primal-Dual Interior Point Method for Smooth Convex Placement Problems

Kennings, Andrew A., *Ryerson Polytechnic University* and Frazer, Mark J. and Vannelli, Anthony, *University of Waterloo*

We present a primal-dual interior point method (IPM) for solving smooth convex optimization problems which arise during the placement of integrated circuits. The interior point method represents a substantial enhancement in flexibility verses other methods while having similar computational requirements. We illustrate that iterative solvers are efficient for calculation of search directions during optimization. Computational results are presented on a set of benchmark problems for an analysis of the method.

TAA15-17 -- An Initial Placement Algorithm for 3-D VLSI

Michiroh, Ohmura, *Hiroshima Institute of Technology*

As manufacturing technology has advanced in recent years, a 3-D IC in which circuits are piled on top of each other has been the focus of attention in the device area. However no initial placement technique has been researched in the layout design of 3-D VLSI. In this paper, we propose a 3-D initial placement algorithm which places strongly connected modules close to each other including adjacent layers by introducing the gains for modules. This algorithm also takes account of layer assignment by multiplying a constant k by the distance in the direction of Z.

TAA15-18 -- A Novel Methodology for Power Consumption Reduction in a Class of DSP Algorithms

Masselos, Konstantinos; Merakos, P.; Stouraitis, T.; and Goutis, C.E., *University of Patras*

In this paper a novel approach for low power realization of DSP algorithms that are based on inner product computation is proposed. Inner product computation between data and coefficients is a very common computational structure in DSP algorithms. The proposed methodology is based on an architectural transformation that reorders the sequence of evaluation of the partial products forming the inner products. The total hamming distance of the sequence of coefficients, which are known before realization, is used as the cost function driving the reordering. The reordering of computation reduces the switching activity at the inputs of the computational units. Experimental results show that the proposed methodology leads to significant savings in switching activity and thus in power consumption.

TAA15-19 -- Performance Modeling for System Design: An MPEG A/V Decoder Example

Hocevar, Dale E.; Sriram, Sundararajan and Hung, Ching-Yu, *Texas Instruments Inc.*

This paper describes a system level performance simulation methodology for VLSI system design of complex signal processing devices. This methodology also provides a means for HW/SW co-simulation and co-design. An MPEG audio/video decoder example illustrates this approach. Through this example we demonstrate an extremely fast simulation method that can process multiple frames of MPEG-2 compressed video per minute, and provides the necessary information for developing and evaluating the decoder architecture. This also allows for rapid simulation over numerous test bitstreams. Our methodology allows us to measure many different performance metrics, quickly construct and alter the

simulation model, process actual bitstreams, and generate test cases. A pathway for developing detailed simulation models of the lower levels of the design process is also discussed.

TAA15-21 -- Graph Transformation for Communication Minimization Using Retiming

Sheliga, Michael; Yu, Zhihong, Chen; Fei; and Sha, Edwin H.-M.,
University of Notre Dame

Nested loops are normally the most time intensive tasks in computer algorithms. These loops often include multiple dependencies between arrays that impose communication constraints when used in multiprocessor systems. These dependencies may be between dependent arrays (loop dependencies), or between independent arrays (data dependencies). In this paper, reducing the communication caused by data and loop dependencies for perfect nested loops is explored. It is shown that for a given partition data dependencies may be treated as a specialized form of loop dependencies. Once this is done, previous results on scalable loop tiling can be used to calculate the final total communication. Next, the effects of changing the partition for both loop and data communication are examined. Using these results, the optimal partition for a number of cases are examined. Results are shown which illustrate the efficiency of the system as well as the savings achieved.

TAA15-22 -- Gate to Channel Shorts in PMOS Devices: Effects on Logic Gate Failures

Sayeed, M. Shahen and Mourad, Samiha, *Santa Clara University*

Gate to channel shorts via oxide layer have enormous effect on VLSI circuits and may render devices useless. However, there is no sure way of detecting and locating such faults due to its random nature. In order to test VLSI circuits, a working model is essential in the event a gate oxide short occurs. A model for gate oxide shorts in PMOS transistors is presented in this paper and used to determine the behavior of digital gates in the presence of these shorts. Except when the short resistance is very low, the failure is not detectable by voltage testing and current or delay testing is necessary.

TAA15-23 -- Realistic Delay Modeling in Satisfiability-Based Timing Analysis

Silva, Luis Guerra; Silva, Joao P. Marques; and Silveira, Luis Miguel, *Cadence European Labs/INESC Instituto Superior Tecnico*; Sakallah, Karem A, *University of Michigan*

Circuit delay computation taking into account the existence of false paths represents a significant and computationally complex problem. Existing research work has focused mainly on path sensitization models and algorithms, and on gate and interconnect delay models. Nevertheless, work in these two main areas has evolved separately, and so most path sensitization models and algorithms assume very rudimentary gate and interconnect delay models. In this paper we propose a modeling framework for circuit delay computation as a sequence of instances of propositional satisfiability. This framework is used to capture several path sensitization models under the unit delay model. Moreover, several algorithms for propositional satisfiability are evaluated seeking to illustrate the computational challenges posed by the circuit delay computation problem. Finally, realistic delay models taking into account extracted interconnect delays and fanout data are incorporated into the proposed circuit delay computation framework in order to experimentally evaluate its applicability.

TAA15-24 -- Enhancing Circuit Performance under a Multiple-Phase Clocking Scheme

Hsu, Yaun-chung, *IBM*; Sun, Shangzhi, *Synopsys, Inc.*; Du, David H. C., *University of Minnesota*; and Chu, Xuedao, *Qufu Normal University*

For general synchronous circuits, input and output data are stored in latches or flip-flops which are triggered by the clock signal, so the clock period is a measurement of circuit performance. Previous studies on this issue are restricted by the assumption of triggering all inputs at the same clock phase. We propose a new method to reduce the clock period without the above assumption. The proposed method allows the existence of clock skew and produces a better clock period. The improvement in circuit performance is demonstrated by our experimental results.

TAB6 – Programmabel Logic Devices

Chair: John I. Sewell

University of Glasgow

11:00 am – 12:30pm - Room: Ferrante III

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAB6-1 -- A Three-Dimensional FPGA with an Integrated Memory for In-Application Reconfiguration Data

Chiricescu, Silviu M.S.A. and Vai, M. Michael, *Northeastern University*

The architecture of a 3-dimensional FPGA for reconfigurable computing machines will be described. This FPGA architecture is based on a novel 3-D VLSI circuit technology developed at Northeastern University. A new interconnection scheme as well as a new reconfiguration mechanism feature the architecture.

TAB6-3 -- Design of a 1.0 Ghz 0.6-um 8-Bit CLA Using PLA-Styled All-N-Transistor Logic

Wang, Chua-Chin and Tsai, Kun-Chu, *National Sun Tat-Sen University*

A high speed 8-bit carry-lookahead adder (CLA)using two-phase clocking dynamic CMOS logic with modified non-inverting all-N-transistor (ANT) blocks which are arranged in a PLA design style is presented in this paper. The pull-up charging and pull-down discharging of the transistor arrays of the PLA are accelerated by inserting two feedback MOS transistors between the evaluation NMOS blocks and the outputs. Detailed simulation results reveal appropriate L/W guidelines for the all-N-transistor(ANT) block design. The analysis of the area (transistor count) tradeoff is also provided in this work. The operating clock frequency is 1.0 GHz while the output of the addition of two 8-bit binary numbers is done in 2 cycles. The proposed design methodology is proved to be also suitable for the long adders, e.g., 64-b adders, while the correct output will be ready in 4 cycles if the 64-b adder is composed of hierarchical nine 8-b CLAs.

TAB6-4 -- Thermal Testing on Programmable Logic Devices

Boemo, Eduardo, Garrido, Javier, and Lopez-Buedo, Sergio;;, *Universidad Autonoma de Madrid*

In this work, an FPGA-oriented temperature monitoring scheme is presented. A control circuit enables a ring-oscillator during a short period and measures its output frequency, a magnitude that is a function of the die temperature. Several sensors have been constructed using Xilinx chips, obtaining sensitivities between 17 kHz per °C and 77 kHz per °C. The characterization of self-heating, matching between identical sensors, power supply dependence and detection of signal contentions has also been performed. The usefulness of other chip resources as thermal transducers, like the built-in OSC4 cell or the IOB clamping diodes, has also been verified. The use of ring-oscillators convert the FPGAs in a powerful tool for researchers interested in thermal modeling of integrated circuits. Just the possibility of "moving" a sensor (or an array of them) over the die, in a simple, fast, and inexpensive way, is almost impossible in any other VLSI technology.

TAB13- DSP Implementations — Poster Session

Chair: Keshab Parhi

University of Minnesota

9:00 am – 12:30pm - ***Room: Serra Ballroom Back I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAB13-1 -- 16-Point High Speed (I)FFT for OFDM Modulation

Bertazzoni, Stefano; Cardarilli, Gian Carlo; Iannuccelli, Manuele; Salmeri, Marcello; Salsano, Adelio; and Simonelli, Osvaldo, *University. of Rome "Tor Vergata"*

In this paper we present the implementation of a 16-point (I)FFT ((Inverse) Fast Fourier Transform) with 24-bit complex data precision suitable for OFDM applications. The die measures 3.2 x 3.3 mm2 and is fabricated in double metal 0.7 um ES2 CMOS technology. Our algorithm does not use any multiplier allowing a throughput up to 85 MWord/s and reducing the core area to less than 5 mm2. It is also possible to implement a 256-point (I)FFT using two 16-point devices and a complex multiplier.

TAB13-2 -- Use of the Chinese Abacus Method for Digital Arithmetic Functions

Maloberti, Franco, *University of Pavia; and* Gang, Chen, *Hunan Normal University*

This paper analyses the basic reasons that the Chinese abacus is used to perform arithmetic function as a popular and efficient technique. Proper electronic circuits, based on pass transistor and domino logic, are achieved to realize the same functions as the Chinese Abacus. Simulations with 0.5 µm CMOS technology show that a parallel 8 bit adder can run at 500 MHz. Moreover, a pipeline 8 bit adder and 8 x 8 bit multiplier can run at 1 Ghz and 800 MHz respectively. Also, the compactness of the physical layout leads to a pretty small area for the circuits.

TAB13-3 -- Residue to Binary Number Converters for Three Moduli Set

Wang, Yuke, Swamy, M.N.S., Ahmad, M. O., *Concordia University*

In this paper, residue to binary number converters for the special moduli sets (2n, 2n+1, 2n+2) and (2n-1, 2n, 2n+1) are studied. Errors in previous publications have been pointed out. New and more efficient converters for both special moduli sets are proposed. Larger multipliers in previous methods are replaced by smaller multipliers and adders. The new converters use about one-half of the hardware required by previous methods.

TAB13-4 -- A New Hybrid Low-Latency Serial-Parallel Multiplier

Al-Besher, B.; Bouridane, Ahmed; Ashur, A.S.; and Crookes, D., *The Queen's University of Belfast*

A new low latency most significant bit first (MSBF), hybrid multiplier architecture is presented in this paper. This multiplier architecture requires fewer pipelining latches than the existing multiplier architectures and reduces the clock-speed for every cycle in the multiplication process.

Furthermore, compared with previous MSBF multipliers the initial delay (latency) is also reduced to three cycles, and one 2n-digit product is produced every 2n+3 cycles.

TAB13-5 -- Efficient Prime Factor Decomposition Algorithm and Address Generation Techniques for the Computation of Discrete Cosine Transform

Chau, Lap-Pui, *Nanyang Technological University,* Lun, Daniel Pak-Kong, and Siu, Wan-Chi, *Hong Kong Polytechnic University*

An efficient prime factor algorithm for the Discrete Cosine Transform is introduced. In this approach, we formulate the decomposition directly, by using the proposed input and output mapping, and derive a novel in-place address generation scheme, whilst the formulations in the literature require multiple stages or have to be done via the DFT. This approach requires one output index mapping only while the conventional algorithms require two mappings. Hence, by using the proposed mappings and address generation techniques, less temporary storage is required during the computation. A comparison of the address generation time between our approach and the conventional non-in-place approach is also shown.

TAB13-6 -- A CORDIC Algorithm with Fast Rotation Prediction and Small Iteration Number

Lin, Chun-Fu *Vanguard International Semiconductor Corporation*; Chen, Sau-Gee, *National Chiao Tung University*

This work proposes a new CORDIC algorithm with merits of small number of rotation iterations, fast prediction of rotation sequence suited for parallel and pipelined operations, and fast simple variable scale factor decomposition and compensation. It has a close to the minimum number of 0.8N iterations (including rotation and compensation) of the algorithm, but has the advantage of facilitating parallel and pipelined operations in realization over the latter algorithm.

TAB13-7 -- Efficient Algorithms for Binary Logarithmic Conversion and Addition

Wan, Yi and Wey, Chin-Long *Michigan State University*

Logarithm number system is an attractive alternatives of the conventional number systems when the data need to be manipulated at very high rate over a wide data range. However, the major problem is deriving logarithm and anti-logarithm quickly and accurately enough to allow conversions to and from the conventional number representations. In this paper, efficient algorithms that convert the conventional number representation to binary logarithm representation are proposed. The algorithms adopt a factorization approach to reduce the look-up table size and an nonlinear approximation method to reduce the computational complexity. Simulation results on IEEE single precision (24 bits) conversion are presented, and the conversion requires only one ROM table with 213x26 bits, one with 213x14 bits, and one with 213x5 bits, or a total of 360 kbits. The algorithm can also be adopted for binary logarithmic addition.

TAB13-8 -- High Level Performance Estimation For a Primitive Operator Filter FPGA

Arslan, Tughrul; Eskikurt; Halil Ibrahim; and D.H.Hoerocks, *Cardiff University of Wales*

The increase in complexity of current VLSI-based FPGA arrays has lead to a demand for efficient methods of estimating their performance characteristics at a higher level. This paper describes a technique for speed and area estimation of DSP-based FPGAs, using the example of a Primitive Operator Filter FPGA [1][2], which targets the realization of reduced complexity digital filters. The technique utilizes information about the FPGAs; the constituent elements of its configurable blocks, in our case, adders, shifters, multiplexers and the CMOS technology under consideration. The paper describes the POF FPGA structure, and the development of metrics for speed and area performance estimation. Results are presented which show the efficiency of the estimation technique.

TAB13-9 -- Direct Digital Frequency Synthesis Using a Modified CORDIC

Grayver, Eugene and Daneshrad, Babak *University of California-Los Angeles*

This paper introduces a new approach to direct digital frequency synthesis (DDFS) based on the Coordinate Rotation (CORDIC) algorithm. The modifications to the standard CORDIC algorithm introduced in this paper allow fine frequency resolution, and exhibit significant potential for low power applications. The new architecture does not need a large ROM and can be implemented on a general purpose processor, or on a flexible ASIC architecture.

TAB13-10 -- High - Speed CORDIC Based Parallel Weight Extraction for QRD-RLS Adaptive Filtering

Ma, Jun, and Parhi, Keshab K., *University of Minnesota;* and Deprettere, Ed F., *Delft University of Technology,*

In this paper, a very high-speed CORDIC based parallel weight extraction algorithm for QRD-RLS adaptive filtering is developed using the matrix look ahead technique. The algorithm is based on inverse updating and is pipelined at fine-grain level. The proposed architecture can be operated at arbitrarily high sample rates, and consists of only Givens rotations which can be mapped onto a Jacobi specific dataflow processor. It requires a complexity of O(M*p^2) Givens rotations per sample period, where p is the size of the input data samples, and M is the pipelining level.

TAB13-11 -- Design of Optimum Power Estimator Based on Wiener Model Applied to Mobile Transmitter Power Control

Huang, A. *Helsinki University of Technology/ Zhejiang University*; Tanskanen, J.M.A.; and Hartimo, I.O., *IRC, Helsinki University of Technology*

Estimation of signal power/instantaneous energy requires nonlinear systems. A power estimator based on the Wiener model is proposed in this paper. Its input signal can be complex-valued, e.g., a baseband signal in a communications system, and its output is guaranteed to be positive. It is computationally very efficient as compared to quadratic filters, and allows for a predescribed prediction step required, for example, for application in delay sensitive closed control loops. Two methods of optimum/partial-optimum design are presented. The partially-optimum power estimator is simulated in COSSAP environment as a part of the power control loop of a CDMA mobile radio communication system. The system performance improvements are observed from bit error rate reductions.

TAB13-12 -- An Implementation of a Normalized ARMA Lattice Filter with a CORDIC Algorithm

Shiraishi, Shin-ichi; Haseyama, Miki; and Kitajima, Hideo, *Hokkaido University*

This paper presents a CORDIC (Coordinate Rotation Digital Computer) implementation of a normalized ARMA lattice filter. Since the proposed method uses a simplified CORDIC algorithm it is possible to implement the CORDIC ARMA lattice filter with a reduced amount of hardware. In addition, we propose a method which transforms the CORDIC ARMA lattice filter realized for signal analysis into a signal synthesis filter without an increase in the implementation complexity. Moreover, the proposed filter can identify unknown-input models so that it can be widely used in the digital signal processing.

TAB14- Circuits and Power Systems II — Poster Session

Chair: Krishnaiyan Thulasiraman

University of Oklahoma

9:00 am – 12:30pm - ***Room: Serra Ballroom Back II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TAB14-1 -- A Class of Systems with Symmetric Impulse Response

Vucic, Mladen and Bahie, Hrvoje, *Faculty of Electrical Engineering and Computing*

In this paper a class of system transfer functions based on the impulse response symmetry criterion is presented. The class is obtained using nonlinear optimization procedure. Optimization of the second to tenth order system is executed. The time and frequency domain properties of obtained system or filter class are given and compared to commonly known filter approximations.

TAB14-2 -- The Formulation and Implementation of an Analog/Digital Control System for a 100kW DC-to-DC Buck Chopper

Ashton, R.W.; and Ciezki, John G., *Naval Postgraduate School*; and Mak, C., *Power Paragon, Inc.*

The authors present a description of the design and implementation of an analog/digital controller for a 100kW Ship Service Converter Module that is being used in a reduced-scale requirements, control law, controller modes of operation and validation studies are documented.

TAB14-3 -- Synchronization of Subthreshold-CMOS Chaotic Oscillators

Neeley, John E.; Overman, Charles H.; and Harris, John G., *University of Florida*

This paper reports on the design and chip measurements from synchronous coupled chaotic oscillators operating in subthreshold CMOS. Each uncoupled oscillator is autonomous and generates chaotic signals with three state variables. For commensurate bandwidth, the subthreshold designs utilize currents and capacitors over 200 times smaller than above threshold realizations. The reduced size makes such designs suitable for single-chip VLSI synthesis of circuit topologies that promote chaotic synchronization. Here, we present both asynchronous and synchronous chaotic data from a fabricated chip to demonstrate the viability of subthreshold CMOS for the spatially distributed design of high-order nonlinear systems.

TAB14-4 -- New Mode-Domain Representation of Transmission Line - Clarke Transformation Analysis

Tavares, Maria Cristina, *State University of Campinas*; Pissolato, J.; and Dortela, C.M., *Federal University of Rio De Janeiro*

This paper presents a new model to represent multiphase transmission lines in transient studies, including the frequency dependence of longitudinal parameters. The frequency dependence is represented with synthetic circuits, with a cascade of pi-circuits for each mode. The transformation matrix used for the entire frequency range is the Clarke one. The model is described for three-phase lines. The exact eigenvector of the non-transposed line are analyzed in the frequency domain for some earth resistivity and compared to Clarke components.

TAB14-5 -- New Mode-Domain Representation of Transmission Line for Power Systems and Studies

Tavares, Maria Cristina, *State University of Campinas;* Pissolato, J. and Portela, C.M., *Federal University of Rio De Janeiro*

This paper presents a new model to represent multiphase transmission lines in transient studies, including the frequency dependence of longitudinal parameters. The frequency dependence is represented with synthetic circuits, with one pi-circuit for each mode. The transformation matrix used for the entire frequency range is the Clarke one and as it is a real matrix it is modeled through ideal transformers. The model is described for three-phase lines. An application of the methodology is presented for a 440 kV single three-phase transmission line. The simulations are performed in EMTP. This line model can be implemented in any digital program with R, L, C and transformer components.

TAB14-6 -- Optimal Power Flow in Distribution Networks by Newton's Optimization Method

de Medeiros, Manoel Firmino, *Universidade Federal do Rio Grande do Norte – UFRN*; and Pimentel, Max Chianca, *Programa de Pós-graduação em Engenharia*

This paper describes the mathematical development of an optimal power flow for radial distribution systems of electric energy. The aim of the optimization process is to determine optimum size and location of capacitor banks in primary feeders, looking to minimize costs with peak power losses, energy losses and bank's installation.

TAB14-7 -- Placement of Variable Impedance Devices for Enhancement of Small Signal Stability in Power Systems

Messina, A.Roman; Begovich, O.; and Sanchez, Edgar N., *IPN-Unidad Guadalajara*

This paper presents an efficient analysis and design method, based on the analysis of controllability and observability measures to place variable impedance devices for enhancement of small signal stability in complex power systems. An advanced linear state model of the power system that includes the representation of high-speed thyristor-based control of variable impedance devices is derived. Based on this representation, a numerically stable algorithm is given for computing controllability of critical system modes as a measure of the distance of the linear state representation form the nearest uncontrollable system. This approach is then extended for computing observability. A location index for variable impedance devices is finally defined from controllability and observability measures.

TAB14-8 -- PLD Implementation of Control Algorithms: Design and Validation

Carmeli, S.; Lazzaroni, M.; and Monti, Antonello, *Politecnico di Milano*

After an introduction to the new features of programmable components, the paper discusses the application of such devices to power electronics. The role of these components in the design of modulator is introduced considering both a simple hardware solution and a mixed hardware and software solution. A design methodology is presented and a detailed description of a validation process based on High Level Petri Nets is given. Some application examples complete the discussion.

TAB14-9 -- Time-Domain Analysis for Reflection Characteristic of Tapered and Stepped Nonuniform Transmission Lines

Murakami, Kazuhito; and Ishii, Junya, *Kinki University*

In this paper, we present the time domain analysis using the MCD simulation and the FFT technique for solving the reflection problem of the nonuniform transmission lines. It is shown that the reflected voltage, and the reflection and transmission coefficients for tapered and stepped transmission-line transformers can be effectively calculated by this approach. The simulted results are in closed agreement with the theoretical results.

TAB14-10 -- A Unified Method for the Small-Signal Modelling of Multi-Resonant and Quasi-Resonant Converters

Szabo, Adrian; Kansara, M.; and Ward, E.S., *The Nottingham Trent University*

A method based on the averaging technique for the small-signal modelling of multi-resonant and quasi-resonant dc-dc converters is presented The characteristic functions of the switching devices are defined and are determined using a numeric algorithm for multi-resonant converters and analytic calculations for quasi-resonant converters. The small-signal control-to-output and line-to-output transfer functions are derived. It is shown that the order of the small-signal model of multi-resonant and quasi-resonant converters is the same as that of the conventional pulse-width-modulated converters. Therefore, all classes of converters can be analysed using a unified method and the large body of existing knowledge concerning PWM converters can be extended to multi-resonant and quasi-resonant converters.

TAB14-11 -- The Application of Feedback Linearization Techniques to the Stabilization of DC-to-DC Converters with Constant Power Loads

Ciezki, John G.; and Ashton, R.W., *Naval Postgraduate School*

The authors have devised a nonlinear coordinate transformation for a dc-to-dc buck chopper supplying a constant power load that facilitates pseudolinearization via a nonlinear feedback. A representative design is introduced and detailed simulation validation studies are presented. The extension of the region of local asymptotic stability is confirmed through Lyapunov analysis.

TAB14-12 -- Highly Efficient CMOS Class E Power Amplifier for Wireless Communications

Tu, Steve Hung-Lung; and Toumazou, Chris, *Imperial College of Science, Technology, and Medicine*

A novel high efficiency low voltage CMOS class E power amplifier for wireless communications is presented. The power amplifier operating at 1.8GHz is designed and simulated with a 0.6-um CMOS process. A two-stage power amplifier architecture with a band-rejection filter for first stage driver delivers 24.8dBm of power to the 50- ohm load with a power added efficiency greater than 73% at a supply voltage of 2.5V.

TUESDAY AFTERNOON -- JUNE 2, 1998

TPA1 – Adaptive Signal Processing

Chair: M.N.S. Swamy

Concordia University, Montreal

2:00pm – 3:30pm - ***Room: Colton I***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA1-1 -- A New Adaptive Algorithm for Reducing the Hardware Complexity

Lee, Haeng-Woo, *Byuksung College; and* Cha, Jin-Jong, and Kim, Kyung-Soo, *ETRI*

An adaptive algorithm for reducing the hardware complexity is presented. This paper proposes a modified LMS algorithm for the adaptive system and analyzes its convergence characteristics mathematically. An objective of the proposed algorithm is to reduce the hardware complexity. In order to test the performances, it is applied to the echo canceller, and a program is described. The results from simulations show that the echo canceller adopting the proposed algorithm achieves almost the same performances as one adopting the LMS algorithm. If an echo canceller is implemented with this algorithm, its computation quantities are reduced to the half as many as the one that is implemented with the normal LMS algorithm, without so much degradation of performances.

TPA1-2 -- A New Approach To Least-Squares Adaptive Filtering

Kocal, Osman Hilmi, *Istanbul Technical University*

A new adaptive algorithm , which is different from the gradient based algorithms and the recursive least-squares algorithms, from the point of view of the mathematical basis that it depends on,to be used for least-squares adaptive filtering is proposed.The algorithm is based on iterative solution methods which are used for the solution of linear equations. It is shown that the new algorithm provides an unbiased estimator for optimum Wiener solution. The proposed method is compared to the least mean square (LMS) algorithm and the recursive least squares (RLS) algorithm, considering computational complexity and rate of convergence criterias. It has been observed that the new algorithm has the convergence rate advantage over the LMS and computational complexity advantage over RLS algorithm. On the other hand, the new method combines desirableconvergence characteristics of RLS when the eigenvalue spreadof the correlation matrix of the input signal is not large. It has been shown that the new methods madpr (multiplication and division per recursion) is always much smaller than that of the RLS and smaller than that of the FRLS algorithm , for M is up to 7, where M is the number of the adjustable weights in the algorithm (order of the system).

TPA1-3 -- Effective Algorithms For Regressor Based Adaptive Infinite Impulse Response Filtering

Acar, Emrah, *Carnegie Mellon University;* Arikan, Orhan, *Bilkent University*

To take advantage of fast converging multi-channel recursive least squares algorithms, we propose an adaptive IIR system structure consisting of two parts: a two-channel FIR adaptive filter whose parameters are updated by rotation-based multi-channel least squares lattice (QR-MLSL) algorithm, and an adaptive regressor which provides more reliable estimates to the original system output based on previous values of the adaptive system output and noisy observation of the original system output. Two different regressors are investigated and robust ways of adaptation of the regressor parameters are proposed. Based on extensive set of simulations, it is shown that the proposed algorithms converge faster to more reliable parameter estimates than LMS type algorithms.

TPA1-4 -- Simplified Realization of Cascaded Adaptive Notch Filters Using Complex Coefficients

Nishimura, Shotaro, and Jiang, Hai-Yun, *Shimane University*

In this paper, we present a new structure for complex adaptive IIR notch filter which is useful for the rejection of narrow-band interference from broad-band signals in QPSK communication systems. The proposed structure is based on the direct form first-order complex notch filter using gradient-based

algorithm. By using the proposed first-order section, a new cascaded structure for complex adaptive notch filter has been shown. The results of computer simulation are shown which confirm the theoretical prediction.

TPA2 – Coding of Arbitrarily Shaped Objects Special Session

Chair: Weiping Li

Lehigh University

2:00pm – 3:30pm - Room: Colton II

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA2-1 -- Coding of Arbitrarily Shaped Objects with Binary and Greyscale Alpha-Maps: What can MPEG-4 Do for You?

Ostermann, Joern, *AT&T Labs*

MPEG-4 Visual, that part of the upcoming MPEG-4 standard describing the coding of natural and synthetic video signals, allows the encoding of video objects using motion, texture and shape information. In this paper, the shape coding algorithms and related texture coding algorithms are described. Whereas binary shapes are coded using a context-based arithmetic en-coder with motion compensation, the coding of greyscale alpha maps requires to code the values of the alpha maps inside of the object in addition to the binary shape information. In order to allow for an efficient coding of the texture at the boundary of arbitrarily shaped objects, padding techniques are used in the encoder and decoder.

TPA2-2 -- Predictive Shape Coding using Generic Polygon Approximation

Kim, Jong-il, and Evans, Brian L., *The University of Texas at Austin*

New predictive binary shape coding is introduced employing contour pel matching and residual contour coding schemes. With minimal complexity overhead, the proposed contour pel matching algorithm can be applied to lossless and lossy contour motion estimation by controlling the maximum tolerance parameter d_max. After motion compensation, a sequence of matched and mismatched segments is coded efficiently using one-dimensional reference contour index. The residual mismatched contour segements are further coded by additional polygons until the distortion is less than d_max. We apply the new shape coding technique to QCIF and SIF MPEG-4 binary mask test sequences to satisfy wide range of d_max values. The key contribution of our technique is in lossy shape coding in which the average coding gain is more than 100% over generalized differential chain coding.

TPA2-3 -- Shape Adaptive Wavelet Coding

Li, Shipeng, *Sarnoff Corporation;* Li, Weiping, *Lehigh University;* Sun, Hongqiao, *Vector Vision, Inc.;* and Wu, Zhixiong, *OKI Corporation*

Efficient coding of arbitrarily shaped visual objects is a new functionality of MPEG-4 visual coding standard, compared with MPEG-1 and MPEG-2. This functionality enables content-based interactivity required in many multimedia applications. There are two aspects of coding an arbitrarily shaped visual object. One is to code the shape information of the visual object (shape coding) and the other is to code the pixels in the visual object (arbitrary shape texture coding). Shape adaptive wavelet coding is a technique for efficiently coding the texture information of arbitrarily shaped visual objects. This paper presents this technique as it is used in MPEG-4.

TPA2-4 -- Joint Shape and Texture Rate Control for MPEG-4 Encoders

Vetro, Anthony, and Sun, Huifang, *Mitsubishi Electric ITA;* and Wang, Yao, *Polytechnic University*

This paper describes an algorithm which can achieve a constant bit rate when coding multiple video objects. First, an initial target estimate is made for each object. Based on the buffer fullness, the total target is adjusted and then distributed proportional to the relative size, motion, and variance of each object. Based on the new individual target rates and rate distortion model for coding the texture of each object, appropriate quantization parameters are calculated. After each object is encoded, the texture model parameters for each object are updated, and if necessary, frames are skipped to ensure that the buffer does not overflow. To provide a proper trade-off between spatial and temporal coding, the proposed rate control algorithm switches between a high rate coding mode and a low rate one. In the low rate mode, a mechanism to control the parameters for shape coding is included. Overall, the algorithm is able to successfully achieve the target bit rate, effectively code arbitrarily shaped objects, and maintain a stable buffer level.

TPA2-5 -- Rate-Distortion Optimal Boundary Encoding using an Area Distortion Measure

Melnikov, Gerry, *Northwestern University*

In this paper an optimal boundary encoding algorithm in the rate-distortion sense is proposed. Second-order B-spline curves are used to model object boundaries. An additive area distortion measure between the original boundary and its approximation is employed in the optimization process. The

problem is formulated in a Directed Acyclic Graph (DAG) paradigm, and the shortest path solution is used to optimally select control point locations of the B-spline curve approximation, based on the desired rate-distortion trade-off.

TPA3 – Neural Networks II: Implementation Issues

Chair: Gert Cauwenberghs

John Hopkins University

2:00pm – 3:30pm - Room: Colton III

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA3-1 -- Continuous-Time Feedback in Floating-Gate MOS Circuits

Hasler, Paul; Diorio, Chris; and Minch, Bradley A., *Georgia Institute of Technology*

We present the negative- and positive-feedback circuit configurations of continuous-time floating-gate MOS circuits. We start by reviewing the dynamics of our pFET and nFET single-transistor synapses. We present the range of possible stabilizing and destabilizing types of feedback in circuits with one floating-gate synapse, including data from nFET and pFET synapses.We then show examples of competitive and cooperative behavior in multiple-synapse circuits. We present experimental data from circuits fabricated in the2um nwell Orbit CMOS process available through MOSIS.

TPA3-2 -- An Analog Neural Network Circuit with Simultaneous Perturbation Learning Rule

Maeda, Yutaka and Kanata, Yakichi, *Kansai University*

In this paper, we describe an implementation of analog neural network system using the simultaneous perturbation learning rule. Compared with usage of the ordinary back-propagation method, we could easily implement the simultaneous perturbation learning rule. The exclusive OR problem and a simple function problem are shown.

TPA3-3 -- A Self-Organizing Map with Resistive Fuse

Kousuke, Katayama; Singo, Kawahara; and Saito, Toshimichi, *Hosei University*

In the paper, we propose a novel SOM algorithm that includes resistive fuse characteristicin order to suppress update of synaptic weights by obstructive inputs.Applying the algorithm to some clustering problems, we have confirmed that the novel algorithm exhibits much better performance than conventional one.We also propose an analog implementation example of the novel SOM and the efficient performance is demonstrated.

TPA3-4 -- Accuracy vs. Precision in General Purpose Neural Digital VLSI Architectures

Alippi, Cesare, *CNR-CESTIA; and* Briozzo, Luciano, *SGS-Thomson Microelectronics*

The paper provides a sensitivity analysis to measure the loss in accuracy induced by perturbations affecting multi-layered perceptrons. Differently from what suggested in the related literature, we do not assume a large number of weights or independence among inputs for the neurons nor again strict requirements on the non linear function. Results are then tailored to digital VLSI implementations where perturbations, caused by quantisation, affect the device inputs, weights, internal values and outputs.

TPA4 – Image and Video Processing II

Chair: Ching-Lin Huang

National Tsing Hua University

2:00pm – 3:30pm - Room: Ferrante I

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA4-2 -- VLSI Implementation of Decoder for Decompressing Fractal-based Compressed Image

Kim, Kyung-Hoon, Hong, Chang-Yu and Kim, Lee-Sup, *Korea Advanced Institute of Science and Technology*

This paper presents an efficient architecture for decompressing fractal-based compressed images and its VLSI implementation with high decoding speed and low hardware cost. The chip is fabricated using 5V, 1 poly 3 metal, 0.6um CMOS technology. The proposed VLSI architecture uses the Modified Recursive Decoding Algorithm(MRDA),which reduces the number of iterations and hardware areas. The proposed decoder architecture shows that RAM size is reduced by 50% and the decoding speed to get final attractor(reconstructed image) is improved by 50%, compared with conventional method using Classical Recursive Decoding Algorithm(CRDA). Based on the operating frequency(50MHz), the decoder can produce about 70~80 image frames(256x256) per second. Therefore, it can decode 2-D quadtree partitioned fractal images in real time.

TPA4-3 -- Fast Integrated Algorithm and Implementations for the Interpolation and Color Correction of CCD-Sensed Color Signals

Kuo, Kuo-Tang,.*ITRI* and Chen, Sau-Gee, *National Chiao Tung University;*

In the traditional design of a CCD sensor*s postprocessing module, one often does interpolations to get all the R, G and B values of a pixel first, followed by other operations, specifically the color correction operations. In this paper, we propose an integrated algorithm for an one-shot operation of combined RGB interpolations and color correction, which reduces computation considerably. Architectural realizations for the new algorithm are also proposed.

TPA4-4 -- Genetic Algorithms for Active Contour Optimization

MacEachern, Leonard A. and Manku, Tajinder, *University of Waterloo*

Genetic Algorithm Snakes (GA-Snakes) are introduced as a new method of contour-based segmentation. The new algorithm exhibits several key features: a low order of complexity, the ability to handle arbitrary constraints, operation in discrete space, avoidance of higher-order derivatives, possible parallel computation, low/fixed storage requirements, the ability to handle large search spaces comfortably, and the ability to escape local minima and to handle non-convex search spaces.

TPA5 – Signal Processing for Communications II

Chair: R. Clark Robertson

Naval Postgraduate School

2:00pm – 3:30pm - ***Room: Ferrante II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA5-1 -- A New Processor Architecture Dedicated to Digital Modem Applications

Monteiro, Fabrice; Philip Serge; Danddache, Abbas; and Lepley, Bernard, *University of Metz*

The aim of this paper is to present a new processor architecture designed to cope with most of the functions of a high rate digital modem application. This work is part of an EURICO European project, whose target is the design of a TV cable modem.

TPA5-2 -- A GSM Modulator Using a Delta-Sigma Frequency Discriminator Based Synthesizer

Bax, Walt T. and Copeland, Miles A., *Carleton University*

This paper describes a new transmitter architecture suitable for GSM modulation. The technique is based on direct modulation of a high resolution delta-sigma frequency discriminator based synthesizer to produce the modulated RF signal without any up-conversion. The advantage of this architecture is that it does not require mixers or D/A converters to generate the In-phase and Quadrature signals as in conventional GSM transmitters. This eliminates many of the analog problems associated with mixing and filtering and results in an architecture suitable for monolithic integration.

TPA5-3 -- Error Resilient Transmission of H.263 Coded Video over Mobile Networks

Lu, Jianhua, Liou, Ming L. and Letaief, K.B., *Hong Kong University of Science & Technology*; and Chuang, Justin C-I, *AT&T Labsh*

In this paper, we propose an error resilient transmission system for reliable transmission of H.263 cdoed video sequence over mobile networks. Both the coded video characteristics and mobile channel statistics are investigated. The error protection schemes are designed based on the best matched block codes coupled with diversity reception. A low complexity error concealment based on prediction of inter-block correlation is also introduced to effectively reconstruct the damaged image blocks caused by the residual errors. Simulations with different test video sequences under various mobile channel conditions confirm that good visual quality can be achieved by the proposed system.

TPA5-4 -- Discrete Fractional Hilbert Transform

Pei, Soo-Chang, and Yeh, Min-Hung, *National Taiwan University*

Hilbert transform plays an important role in the signalprocessing. A generalization of Hilbert transform, wasrecently proposed, and it presents physical interpretation in the definition. In this paper, we develop the discrete fractional Hilbert transform to the edge applications.

TPA6 – Circuits and Systems for Communications Networks I

Chair: Magdi Bayoumi

University of Southwestern Louisiana

2:00pm – 3:30pm - Room: Ferrante III

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA6-1 -- A Low-Power VLSI Design Methodology for High Bit-Rate Data Communications over UTP Channel

Goel, Manish and Shanbhag, Naresh R., *University of Illinois at Urbana-Champaign*

Presented in this paper is a systematic methodology to design low-power integrated transceivers for broadband data communications over unshielded twisted-pair (UTP) channels. The design methodology is based upon two algorithmic low-power techniques referred to as Hilbert transformation and strength reduction and a high-speed pipelining technique referred to as relaxed look-ahead transformation. Finite-precision requirements and power savings are presented. The application of these techniques to design low-power and high-speed 155.52 Mb/s ATM-LAN and 51.84 Mb/s VDSL transceivers is illustrated.

TPA6-2 -- VLSI Design of an ATM Switch with Automatic Fault Detection

Tsui, Chi-Ying, *Hong Kong University of Science and Technology*

This paper describes a VLSI implementation of a multistage self-routing ATM switch fabric. The size of the switch prototype is 16x16 and is designed to handle the OC-12 (622 Mbps) link rate. Based on a bit-slice architecture, the entire 16x16 switch is implemented using four identical chips. The switch has multiple paths, created by a randomizer in front of the routing stages, between each input-output pair. The switch uses an input/output-buffering scheme and contains no buffers inside the fabric. To facilitate fault detection and isolation, we add automatic fault detection schemes at the node, chip, and system levels of the design.

TPA6-4 -- A Signaling Protocol Architecture for an ATM Mobile Simulator

Yoo, Jeong-Ju; Nah, Jae Hoon; Yoo, Jea Hoon; Lee, Yoon Ju, *Electronics and Telecommunications Research Institute*; and Hutchison, David, *Lancaster University*

Our ATM mobile simulator to be presented is implemented on a device as a workstation, which is included mobility functions to be interacted with an ATM switching controller. In this paper, we summarized how to easily implement mobile signaling protocol of the ATM mobile simulator to verify mobility functions of an ATM mobile switching controller. A basic functional model is proposed in association with mapping the model onto our simulator. This paper also presents the signaling protocol stack and signaling protocol procedure for our ATM mobile simulator in order to support mobile terminal access, bearer control and call control.

TPA7 – Analog VLSI

Chair: Yoji Kajitani

Tokyo Institute of Technology

2:00pm – 3:30pm - Room: Bonzai I

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA7-1 -- Mutual Synchronization in 4 Coupled Oscillators with Different Natural Frequencies

Moro, Seiichiro; Mori, Shinsaku; and Sasae, Iuao, *Fukui University*

In this paper, we investigate the synchronization phenomena in 4 oscillators with different natural frequencies full-coupled by capacitors. When there is no natural frequency difference among the oscillators, 4-phase oscillation is not stable. In this system, however, because the frequencies of the oscillators have a slight difference, nearly sinusoidal 4-phase oscillations are stably excited. Moreover we have proved the stability of 4-phase solutions by calculating the stability of the fixed points and considered why frequency locking occurs. From the results we can confirm that 4-phase oscillations can be excited when the symmetry of the system collapses.

TPA7-2 -- Short Period Oscillations from a Sigma-Delta Modulator

Davies, Anthony Christopher, *King's College London*

A method is given to derive existence conditions for short-period oscillations which can occur in the zero-input behaviour of a sigma-delta modulator structure incorporating a third order direct-form digital-filter. The approach is limited in practice to short periods and low-order digital filters because of the complexity of the symbolic and numerical analysis involved. However, short-period oscillations give rise to narrowband 'tones' in the output spectrum of SD modulators, and their understanding and elimination is important for practical applications. The method is explained with simple examples.

TPA7-3 -- Spatiotemporal Dynamics of a Stochastic VLSI Array

Neff, Joseph Daniel; Patel, Girish N.; Menders, Brian; DeWeerth, Stephen P.; and Ditto, William L. *Geogia Institute of Technology*

In this paper we present an analog VLSI array of hysteretic elements that facilitates the exploitation of known properties of stochastic resonance. We present data from a 7x9 array of locally coupled Schmitt trigger elements implemented in a 2µM n-well process. In particular, we demonstrate stochastic resonance in a single element (uncoupled case) with an improvement in output signal to noise ratio of approximately 40 dB. In a spatially extended system (elements coupled via analog transmission gates), we observe an array enhanced effect by measuring the relative firing times between two cells in the array.

TPA7-4 -- IC Implementation of a Current-Mode Chaotic Neuron

Herrera, Ruben D.;Suyano, Ken; and Horio, Yoshihiko, *Columbia University*

An IC implementation of a new current-mode chaotic neuron is presented. The circuit mainly consists of CMOS inverters, which are used as transconductance amplifiers and nonlinear elements. The chip was fabricated using 1.2 um HP CMOS process. One neuron occupies only 0.0076 mm^2, which is smaller than a standard bonding pad. The circuit was tested at a clock frequency of 2 MHz.

TPA9 – Communicating with Chaos Special Session

Chair: Michael Peter Kennedy

University College Dublin

Organizer: Michael Peter Kennedy

University College Dublin

Geza Kolumban

Technical University of Budapest

Sponsor: Technical Committee on Nonlinear Circuits and Systems

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2:00pm – 3:30pm - Room: Bonzai III

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA9-1 -- Communicating via Chaos Synchronization Generated by Noninvertible Maps

Millerioux, Gilles and Mira, Christian, *Institut National des Sciences Appliquées*

This paper deals with chaos synchronization for secure communications, the chaotic signals being generated by piecewise linear noninvertible maps. With respect to the solutions described till now, such maps permit specific dynamic features improving significantly the system characteristics. Chaos synchronization is obtained by introducing an observer model. Here the purpose is to illustrate some of these characteristics from a very simple example, using results proved previously in the general case.

TPA9-2 -- From Chaotic Maps to Encryption Schemes

Kocarev, Ljupco and Jakimoski, Goce, *"Sv. Kiril i Metodij" University*; Stojanovski, Toni, *RMIT University;* and Parlitz, Ulrich, *Universitat Gottingen*

Relationship between cryptography and chaos theory, and similarities of their crucial concepts such as: mixing property, and sensitivity to changes in initial conditions and parameters are explained. An example of an encryption algorithm based on chaotic maps is presented.

TPA9-3 -- Chaotic versus Classical Stream Ciphers - A Comparative Study

Dachselt, Frank, *TU Dresden*; Kelber, Kristina; Schwarz, Wolfgang; Vandewalle, Joos, *KU Leuven*

Chaotic and classical (binary) stream ciphers are compared with respect to their cryptographical properties. Possible synchronization schemes, algebraic and analytical properties as well as design and implementation aspects are discussed. For two example classes with similar system structures it is shown that chaotic stream ciphers can achieve a higher level of complexity than classical binary systems due to the algebraic properties of the system structure.

TPA9-4 -- Some Tools for Attacking Secure Communication Systems Employing Chaotic Carriers

Ogorzalek, Maciej J., *University of Mining and Metallurgy;* and Dedieu, Herve, *Swiss Federal Institute of Technology*

We present a review of methods which can be used to uncover the information signal hidden using one of so-called chaos communication methodologies. All of the known secure communication methods employing chaotic carriers are shown to be of very low security.Hidden messages can be found using extremely simple reasoning and straightforward computational methods. We point out also that none of the methodologies proposed so far uses properties of chaotic signal. The only property exploited is the sensitivity (instability) of the transmitter/receiver pair to parameter and initial condition changes.

TPA10 – Circuit Simulation

Chair: Michel Nakhla

Carleton University, Canada

2:00pm – 3:30pm - ***Room: San Carlos I***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA10-1 -- Applications of the Variable Dimension Newton Method to Large Scale Circuits

Ng, Shek-Wai, *Hong Kong Polytechnic University*

The Variable Dimension Newton Method (VDNR) is used to solve the DC solutions of various kinds of circuits. The problems encountered and the corresponding solutions are discussed. The simulation results show that the Variable Dimension Newton Method is much robust than the conventional Newton method and those homotopy alternatives used in SPICE3f3.

TPA10-2 -- HomSPICE: Simulator with Homotopy Algorithms for Finding DC and Steady-State Solutions of Nonlinear Circuits

Trajkovic, Ljiljana, *Simon Fraser University*; Fung, Eula; and Sander, Seth, *University of California - Berkeley*

We describe the use of homotopy (also called parameter embedding and continuation) methods for finding dc operating points and steady-state solutions of BJT and MOS transistor circuits. Past implementation of homotopy algorithms in proprietary industrial circuit simulators proved that they were viable options to resolving convergence difficulties for finding circuits' dc operating points. In this paper we describe a software implementation of publicly available homotopy algorithms (from the software package called HOMPACK) in the UCB SPICE circuit simulator. The new simulator, called HomSPICE, provides options for finding a circuit's dc operating points and steady-state solutions via three homotopy algorithms. We illustrate the performance of HomSPICE on several simulation examples.

TPA10-3 -- Convergence Conditions of Waveform Relaxation Methods for Circuit Simulation

Jiang, Yao-Lin, *Xian Jiaotong University*; and Wing, Omar, *The Chinese University of Hong Kong*

For two general classes of circuits which are described by nonlinear differential-algebraic equations and linear differential-albegraic equations, respectively, we present convergence conditions of the waveform relaxation methods, in which the proofs are based on the operator spectral theory and are identical. These convergence conditions reveal the types of splittings of the equations for which the waveform relaxation methods will converge.

TPA10-4 -- A Time-Frequency Algorithm for the Simulation of the Initial Transient Response of Oscillators

Brachtendorf, H.G., *Bell Labs*; and Laur, Rainer A., *University of Bremen*

The paper presented here deals with a novel algorithm for calculating the initial transient response of an oscillator circuit. The method is based on reformulating the original system of ordinary differential-algebraic equations (DAEs) by a system similar to partial differential equations (PDEs). The time-scales of the solution of the PDEs are unlike the original DAEs not widely seperated. The PDE approach is therefore much better suited for CAD. Unlike existing methods the novel algorithm has a sound mathematical basis.

TPA11 - Robotics

Chair: David C. Jenn

Naval Postgraduate School

2:00pm – 3:30pm - Room: San Carlos II

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA11-1 -- Wireless Power Transfer for a Micro Remotely Piloted Vehicle

Jenn, David, *Naval Postgraduate School*

A prototype rectifying antenna (rectenna) to provide wireless power transfer (WPT) to a micro-remotely piloted vehicle (MRPV) is developed. Microwave radiation at 1.3 GHz is converted into DC to drive a small motor and spin a mockup helicopter rotor blade. The rectenna serves a dual purpose as the antenna and outer body of the proposed vehicle and allows efficient reception of power over 360 degrees around the vehicle. Wireless power transfer to the mockup MRPV has been demonstrated with less than 1 watt of transmitted power at near field ranges. Rectification efficiencies up to 30% were measured for two rectifier circuit configurations using 1.3 GHz continuous wave (CW) and pulse modulated transmitted signals.

TPA11-2 -- Sliding Mode Control for Elastic Multi-Link Manipulators based on the Dynamic Compensation Method

Utkin, Victor A., *Institute of Control Sciences*

The paper introduces a sliding mode control design for the tip position tracking of a multi-link flexible manipulator based on the method of dynamic compensation. The controller in vibration control of a flexible structure is, usually, developed only on the basis of a finite number of modes, which are called the rigid-body coordinates. The remaining high frequency modes describe the behavior of vibrations inherent to elastic arms called the flexure coordinates. As a rule, the rigid-body coordinates and/or the tip position can be measured directly. The design approach suggested here can be realized by three independent stages. First, the sliding mode is generated in the subsystem, which describes the rigid body motion, with the aim to guarantee tracking error convergence of the manipulator tip motion. At this design stage the link flexure is treated as the disturbances. In the next stage of design procedure the dynamic compensator is selected to obtain the indirect estimation of flexure coordinates, Note, that the state vector of dynamic compensator converges to values of flexure coordinates under condition of the of sliding mode motion occurrence in the rigid-body coordinate subsystem. In the third stage, the algorithm to be developed to provide the desired damping ratio of the flexure coordinates subsystem. The possibility of parametric damping is also considered. Finally, the procedure of design problem taking into account the dynamic joint actuator is presented.

TPA11-3 -- New Broadband 100-MBPS Switch System Using Broadband Pin-Board Switch and High-Precision Pin-Handling Mechanism

Inagaki, Shuichiro, *NTT Opto-electronics Laboratories*

A broadband pin-board switch system using high-precision pin-handling technology was studied. It can crossconnect 320 twisted pair cables with 240 twisted pair cables. Experiments showed that the error rates of the system applied to a 100-Mbps Fast Ethernet LAN and a 150-Mbps ATM LAN meet the criteria of the LAN links.

TPA11-4 -- An Agent-Based Structure for Mobile Robots Using Vision and Ultrasonic Sensors

Bastos-Filho, Teodiano Freire; Freitas, Roger Alex de Castro; Sarcinelli-Filho, Mario, and Schneebeli, Hansjorg Andreas, *Federal University of Espirito Santo - UFES*

Object recognition is an important task associated to mobile robots navigation. Upon detecting any obstacle, the recognition system must be able to say which obstacle is in the robot trajectory, so that the control system is able to plan a new trajectory for the robot, deviating from the detected obstacle or following it, depending on which is the obstacle. It is normally necessary to recognize a few obstacles that are commonly present in the robot operating environment. In this paper, a system is proposed to perform the task of recognizing the objects present in the trajectory of a mobile robot. This system is based on information coming from ultrasonic sensors and a digital monochromatic camera. The operation of this system is addressed, as well as an example of object detection and recognition is presented.

TPA12 – Feedback Systems and Stability

Chair: Bell A. Shenoi

Wright State University

2:00pm – 3:30pm - ***Room: San Carlos III***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA12-1 A -- General Operating-Point Instability Test Based on Feedback Analysis

Fox, Robert M., *University of Florida*

A general test is presented for detecting unstable dc operating points, extending and simplifying previous nresults. Signal-flow-graph concepts illustrate how familiar feedback analysis methods can greatly simplify the required analyses.

TPA12-2 -- A 3.3V all Digital Phase-Locked Loop with Small DCO Hardware and Fast Phase Lock

Chiang, Jen-Shiun, *Tamkang University*; and Chen, Kuang-Yuan, *Key Tech Corporation*

This paper is to design and implement an all digital phase-locked loop (ADPLL) circuit. The core of the ADPLL is the switch-tuning digital control oscillator (DCO). Our design of the DCO has features of small hardware cost. This ADPLL has characteristics of fast frequency locking, full digitization, easy design and implementation, and good stability. It is suitable to be used as the clock generator for high performance microprocessors. A prototype of this ADPLL chip is designed and implemented by TSMC¡¦s 0.6um SPDM CMOS process. The simulation shows that this chip can operate in the range between 60MHz and 400MHz, and operates at 4x the reference clock frequency. The phase lock process is 47 clock cycles, and the phase error is less than 0.1ns. The chip consists of 4026 MOS transistors and the core size of the VLSI layout is 923umx921um.

TPA12-3 -- A Novel Algorithm that finds Multiple Operating Points of Nonlinear Circuits Automatically

Goldgeisser, Leonid; and Green, Michael M., *University of California, Irvine*

The use of continuation methods has been shown to be more effective than standart Newton-Raphson based methods in finding the operating point(s) of circuits with convergence problems. In this paper a new algorithm that searches for multiple operating points automatically, with no user intervention required, is shown to be a direct extension of the use of a particular continuation method. This algorithm, which exploits the assymetrical properties of nonlinear mappings that describe multistable circuits, has been implemented into a program which automatically finds multiple (in most cases all) operating points of a circuit. A number of challenging examples are given.

TPA12-4 -- An Extension of the Classical Feedback Theory

Neag, Marius; and McCarthy, Oliver, *University of Limerick*

The classical feedback theory (CFb theory) is a useful tool for circuit analysis but has some limitations: it deals with one-input one-output circuits only; in order to simplify the calculations the signal fed forward by the feedback network is usually neglected but a thorough analysis of the resulting errors is not provided. Moreover, it supplies a degree of traditionalism in the feedback circuits' analysis and design. This paper presents an extension of the CFb theory that provides a unitary approach to the analysis of feedback circuits, dealing with both voltage and current as input and output signals. The new analysis method is not more difficult to use than the classical one and it spotlights the elements that control the circuit parameters, such as the ideal closed loop gain and the bandwidth. The method was verified by comparison with a direct analysis, at Kirchhoff's laws level, for circuits having a Pi and a T feedback network. Thus its validity was demonstrated for any reciprocal two-port feedback network; also, an estimation of its errors when compared with the direct (i.e. accurate) analysis is provided.

TPA13 – Multimedia Processing Poster Session

Chair: Che-Ho Wei

National Chaio Tung University

Chair: Yeong Ho Ha

Kyungpook National University

2:00pm – 3:30pm - Room: Serra Ballroom Back I

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA13-1 -- An LPC Cepstrum Processor for Speech Recognition

Hwang, In-chul; Kim, Sung-Nam; Kim, Young-Woo; and Kim, Soo-Won, *Korea University*

An LPC cepstrum processor for speech recognition is implemented on CMOS gate array. The processor that we designed contains a 24 bit floating-point MAC unit, which computes a correlation rapidly, the majority of operations in the algorithm. This processor has 22 register files to store temporary variables, which enable to reduce access to external memory. For the purpose of fast operations, the floating-point MAC consists of a pipeline structure with 3 stages and uses a branched postnormalization scheme proposed in this paper. Experimental results show that it takes approximately 266 us to process a frame of 20 ms at 15 MHz clock rate. This processor runs at the maximum rate of 16.6 MHz and the number of transistors is 55,520.

TPA13-2 -- A Visual Model for Subband Image Coding

Fong, W.C., Chan, S.C., and Ho, K.L., *The University of Hong Kong*

In this paper, we propose a visual model for the general subband coding system. This model is a generalization of Watson's visual model for DCT. Based on this model, a new perceptual distortion is proposed which can be used together with an efficient bit allocation algorithm to determine the quantizer stepsizes of subband coders. Simulation results and subjective viewing tests demonstrate that the proposed approach is very effective in improving the subjective quality of the encoded image at low bit rate.

TPA13-3 -- A Fast and Accurate Scoreboard Algorithm for Estimating Stationary Backgrounds in an Image Sequence

Lai, Hon Seng and Yung, Nelson, *The University of Hong Kong*

This paper presents a stationary background estimation algorithm for color image sequence. The algorithm employs the running mode and running average algorithms, which are two commonly used algorithms, as the estimation core. A scoreboard is used to kept the pixel variations in the image sequence and is used to select between the running mode or the running average algorithm in each estimation. Our evaluation results show that by selecting, intelligently, the estimation core between the two algorithms according to the scoreboard values, the proposed background estimation algorithm has excellent performance in terms of estimation accuracy and speed.

TPA13-4 -- Subimage Error Concealment Techniques

Hasan, Moh'd Abdel Majid, *AMIEE*, Sharaf, Atif Ibrahim and Marvasti, Farokh I.*King's College, MIEEE*

Images transmitted via ATM networks suffer from quality degradation due to buffer overflow or cell header errors which cause ATM cells to be lost. This paper presents a new approach to conceal the errors in the received images by the application of novel error recovery techniques to the decomposed DCT-coefficient subimages of the corrupted image. These techniques were developed to recover images corrupted by impulsive noise. Since decomposing the corrupted image into the DCT-coefficient subimages generates low resolution images corrupted by impulsive noise, all the techniques used to recover images corrupted by impulsive noise can be used to recover the subimages and hence the corrupted image. In this paper, we study the performance of different iterative and non-linear techniques to recover the corrupted subimages. The quality of the recovered image using these techniques is better than the quality obtained by many classical error concealment techniques.

TPA13-5 -- Wipe Scene Change Detector for Segmenting Uncompressed Video Sequences

Alattar, Adnan Mohammed, *King Fahd University of Petroleum & Minerals*

The use of wipes in video production to smooth the transition between two consecutive scenes complicates subsequent video compression, video editing, and video database indexing. It is important to detect the wipe region in order to improve the quality of the compressed video or to allow automatic parsing of the video for the purpose of editing and data base indexing. In this paper, a model is developed for the wipe region and is used to derive the statistical characteristics of the frames in the wipe region. A wipe detector that exploits the linear change in the means and the variances of the frames in the wipe region is developed. The developed wipe detector is implemented and tested with video sequences containing wipes of different types and lengths. Simulation results indicate that wipe regions are well represented by the developed wipe model, and that the

developed wipe detector is robust to wipe type and length.

TPA13-6 -- Hierarchical Scene Change Detection in an MPEG-2 Compressed Video Sequence

Shin, T, *Kwangju Institute of Science & Technology*; Kim, J.G. Lee, H. and Kim, J., *Electronic and Telecommunications Research Institute*

In this paper, we propose an efficient scene change detection algorithm for direct processing of mpeg-2 video bitstreams. the proposed algorithm utilizes the hierarchical structure of the compressed bitstreams and statistical characteristics of the coded parameters, thus greatly reducing computational requirement compared to pixel domain processing with full decompression. occurrence of scene change is checked first in a gop level, and if the result is affirmative it is checked again in lower levels : sub-gop and each picture. we used several metrics for different levels : variance of dc images for i-pictures, number of macroblock types for p-pictures and motion vector types for b-pictures.

TPA13-7 -- A Robust Linear Prediction Method For Noisy Speech

Shimamura, Tetsuya, Kunieda, Nobuyuki and Suzuki, Jouji. *Saitama University*

This paper proposes a method to improve the performance of the LP method in a noisy environment. A relationship for the autocorrelation function (ACF) of a periodical signal is derived, and the ACF estimates of noisy speech are transformed into their noiseless ones. The normal equation in which the noiseless ACF is used is efficiently solved by the Levison-Durbin algorithm. Computer simulations demonstrate that the proposed method provides and improvement in the LPC cepstrum distance.

TPA13-8 -- Object Tracking and Hypermedia Links Creation in MPEG-2 Digital Video Sequences

Favalli, Lorenzo; Mecocci, Alessandro; and Fulvio, Moschetti, *University of Pavia*

The work presented in this paper, describes a tool for object tracking, notes insertion and information retirval to be applied to MPEG-2 sequences. Maximum compliance with the MPEG standard is sought, in that the added information is transmitted as side information without affecting the actual video-audio stream that can be decoded by a standard MPEG-2 decoder. Additional processing is added to a standard encoder only with the scope to allow the automatic tracking of one object across different Groups of Pictures which would otherwise be unrelated. Results show that the proposed algorithm is capable to track objects with a good degree of precision for about 100 frames. Features are included to allow the identification of objects even after occlusions, provided that some (reasonable) restrictions are met.

TPA13-9 -- Syntax Based Error Concealment

Papadakis, Vasilios, Lynch, William E. and Le-Ngoc, Tho, *Concordia University*

We study error control for an MPEG2 digital video compression scheme. We propose to combine error control coding together with error concealment. Classical error detection is used to locate errors in the compressed video bitstream. This information, together with information provided by the syntax of the compressed bitstream, is used to perform the error concealment. Thus the concealment is performed in the compressed video domain. The introduction of a new concealment method which relies on the redundancies that the syntax of the compressed bitstream provides, is the main contribution of this work. Another contribution is the performance evaluation between the proposed scheme, a general error correction scheme, and a simple case, where no effort is made to correct existing errors.

TPA13-10 -- Digital Restoration of Painting Cracks

Giakoumis, Ioannis and Pitas, Ioannis, *Aristotle University of Thessaloniki,*

In this paper we develop a method for the restoration of cracks on a painting. First, we detect the local minima (they can be either cracks or painting brush strokes), by using a morphological high-pass operator, called top-hat transformation. The crack filling procedure must be applied only on the cracks and not on these dark brush strokes, which are also detected. In order to separate these brush strokes from cracks, we use the Hue and Saturation information in the HSV or HSI color space. The separation is obtained by classification through the implementation of the MRBF neural network. Alternatively, a semi-automatic method is described for this separation. The primitive geometric shape-matching property of the morphological opening can be used to separate brush strokes, which have a specific shape. Finally, we propose two crack filling methods, one which is based on order statistics and another one using anisotropic diffusion. The results on painting crack restoration were very good.

TPA14: Oversampled and Sigma-Delta Techniques — Poster Session

Chair: Terri Fiez

Washington State University

2:00pm – 3:30pm - ***Room: Serra Ballroom Back II***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA14-1 -- Harmonic Distortion in Switched-Current Sigma-Delta Modulators due to Clock Feedthrough

Martins, J. M., and Dias, V. F., INESC

Harmonic distortion induced by the clock feedthrough in Switched-Current Sigma-Delta modulators is discussed. An expression is derived for the level of the second harmonic as a function of the parameters of the integrators. The results indicate that the level of the 2nd harmonic at the modulator output can be reduced with respect to that of SI cells and integrators by a factor of approximately the oversampling factor. SPICE simulations that confirm the results obtained have been performed using a special technique to take into account accurately the clock feedthrough effects.

TPA14-2 -- Analysis of Non-Uniform Sampling Effects in Sigma-Delta Modulated Signals

Lee, Eel-Wan, and Chae, Soo-Ik, Seoul National University

The effects of non-uniform sampling in the Sigma-Delta modulated DAC are discussed in this paper. The non-uniform sampling of the Sigma-Delta modulated signals causes in-band noises in the DAC, which will be compared with the harmonic distortions in switched capacitor circuit and that due to the signal-dependent nonlinearity in the 1-bit DAC. We describe an error-driven edge selection algorithm that suppresses the in-band noise and its implementation. We also propose a model of the in-band noise caused by the non-uniform sampling, which predicts the reduction of the spectral shaping in the frequency domain quantitatively based upon the transition probability of the modulator output.

TPA14-3 -- New Analytical Model of Interpolation Waveforms in Time-averaging Interpolative Digital to Analogue Convereters

Moniri, Mansour, *Staffordshire University*

This paper introduces a new analytical model for the study of interpolation waveforms in time-averaging interpolative digital to analogue converters (DACs). This analytical model reveals some important phenomena about the interpolation process and can be used to determine the effects of varying individual interpolation waveforms on the overall performance of DACs. This allows strategies to be developed for minimising interpolation noise and can also be used to enhance the performance of large number of interpolation schemes.

TPA14-4 -- Encoding Hidden Data Channels in Sigma Delta Bitstreams

Sandler, Mark B., and Magrath, A.J., *King's College London Koszalin*

A new technique is introduced which allows a hidden data channel to be encoded onto a sigma-delta bitstream in addition to the primary signal input. The technique is developed so that the primary signal can be demodulated by standard techniques, without interference by the side channel. Applications include imprinting a watermark onto an archived audio recording, or encoding additional hidden audio or video channels in the bitstream. Results are presented which indicate that side-channel data rates in excess of 500 kbit/sec are possible

TPA14-5 -- An Architecture of Delta Sigma A-to-D Converters Using a Voltage Controlled Oscillator as a Multi-Bit Quantizer

Iwata, Atsushi, Sakimura, Noboru, Nagata, Makoto, and Morie, Takashi, *Hiroshima University*

This paper proposes a new architecture for an oversampling Delta-Sigma Analog-to-Digital converter utilizing a voltage controlled oscillator (VCO), called a VCO DS A-to-D converter. The converter consists of a VCO, a counter, an analog integrator, and a feedback D-to-A converter. Through functional and circuit simulations, an SNR of over 50dB was obtained at a 5MHz signal bandwidth and 400MHz sampling frequency using 0.6µm CMOS technology. This architecture is highly suitable for implementation with deep sub-um CMOS devices that can attain improved switching speeds and reduce power dissipation during low voltage operation. It provides wideband oversampling A-to-D converters for video and wireless signals and a low volateg system-on-a-chip solution for multi-media applications.

TPA14-6 -- Current Mode Approach To Sigma-Delta Modulators

Wawryn, Krzysztof, and Suszynski, Robert, *Technical University of Koszalin*

The paper presents an approach to sigma-delta modulators relying on current mode sampled data circuits with switched transconductances. The sigma-delta modulator structures are composed of current mode building blocks with transconductance amplifiers and capacitors. All building blocks and three different sigma-delta structures: first-order, second-order and multistage are designed and simulated by using VLSISPICE COMPASS DESIGN programs on SUNSPARC20 computer and then manufactured via Eurochip service center in 0.7um ES2 digital process to verify proposed concept. The multistage sigma-delta modulator perform 11 bit resolution over the frequency band at 3.3V power supply. Presented results of noise shaping function, dynamic range and power consumption of sigma-delta modulators prototypes demonstrate that the technique of switched transconductances can considered as a valid realization of sigma-delta modulators and an alternative to the SC and standard SI techniques.

TPA14-7 -- A Folding ADC Employing a Robust Symmetrical Number System with Gray-Code Properties

Pace, P.E., *Naval Postgraduate School*, and Styer, D., *University of Cincinnati*, and Akin, I.A., *Naval Postgraduate School*

A folding analog-to-digital converter (ADC) preprocessing design based on a new robust symmetrical number system (RSNS) is presented. The RSNS preprocessing architecture is a modular scheme in which the integer values within each modulus (comparator states), when considered together, change one at a time at the next position (Gray code properties). Although the observed dynamic range of the RSNS ADC is somewhat

less than the optimum symmetrical number system ADC, the RSNS Gray code properties make it particularly attractive for error control. With the RSNS preprocessing, the encoding errors due to comparator thresholds not being crossed simultaneously are eliminated. As a result, the interpolation circuits can be removed and only a small number of comparators are required. Computer generated data is used to help determine the properties of the RSNS. These properties include the dynamic range (largest number of distinct consecutive vectors) and the location of the dynamic range within the number system. Closed-form expressions for the dynamic range are also presented for channel moduli of the form m1 = 2k -1, m2 = 2k, m3 = 2k + 1. To compare the advantages of the RSNS ADC with previously published results, the transfer function of a 3-channel architecture (k=2) is evaluated numerically using SPICE.

TPA14-8 -- Performance Analysis of Low Oversampling Ratio Sigma-Delta Noise Shapers for RF Applications

Gothenberg, Andreas, and Tenhunen, Hannu, *Royal Inst. of Technology*,

Baseband signal processing for current base stations or 3rd generation mobile systems will impose high bandwidth and high VLSI integration demand. Many of the desired integration aspects can be satisfied with sigma-delta converter front-ends. However, under the technology constraints there are simultaneous requirements for high sample rate and low oversampling ratio in order to achieve the desired baseband width. In this paper, we present system architecture results for 4th-order cascaded noise shaper architectures for baseband front-ends and show that the cascaded structures with proper scaling will satisfy simultaneous demand on linearity (spurious free dynamic range) and high SQNR with low oversampling ratio based on usage of multibit quantizers outside the actual signal noise shaping path.

TPA14-9 -- Adaptive Compensation of Analog Circuit Imperfections for Cascaded Delta-Sigma ADCs

Sun, Tao, *Oregon State University*

Cascaded delta-sigma modulators are known to suffer from analog circuit imperfections. The adaptive algorithm and structure proposed in this paper can digitally compensate the effects of these imperfections using digital filtering. Experimental results show that after compensation a performance improvement of more than 25 dB in signal-to-noise-and-distortion ratio can be achieved.

TPA14-10 A -- Two-Loop Third-Order Multistage Delta-Sigma Frequency To Digital Converter

Filiol, Norman M.,*Carleton University*,

This paper presents a delta-sigma frequency to digital converter based on two delta-sigma PLLs.A primary delta-sigma PLL performs frequency discrimination with first order noise shaping while a secondary delta-sigma PLL performs a second order noise shaped measurement of the quantization phase error introduced by the primary PLL. Then, as in multistage A/D converters, the two digital outputs are combined to produce a cancellation of the quantization phase-error introduced by the primary PLL. This paper presents results from a hardware prototype following the above concept, built with discrete ECL components. Measured results indicate that the circuitcould function as a highly linear FM demodulator from an IF frequency or alternatively could form part of a frequency synthesizer. The secondary delta-sigma PLL which provides the noise-shaped phase error appears to be new. Its application to frequency synthesis is also discussed.

TPA14-11 -- An Oversampled A/D Converter Using Cascaded Fourth Order Sigma-Delta Modulation and Current Steering Logic

Miao, Guoqing, *Crosslink Semiconductor, Inc.*, and Yang, Howard C., *Newave Semiconductor Corp.*, and Tang, Pushan, *Fudan University*

In this paper the design and measured results of a 4th order sigma-delta A/D converter is presented. Signal scaling technique was used to alleviate its large signal overload problem and maximize the allowable input signal level, which also increases the maximum output SNR. A low noise current steering logic was used to design the digital noise cancellation logic, which reduces the digital coupling noise and simplifies the circuit layout. The experimental chip was fabricated with a 3um CMOS technologyand operated from a single 5V power supply. With an oversampling ratio of 64, it achieves 91dB dynamic range and 50kHz conversion speed. The peak SNR is 88dB.

TPA14-12 -- A 12-bit, 100ns/b, 1.9mW CMOS Switched-Current Cyclic A/D Converter

Wey, Chin-Long, and Wang, Jin-Sheng, *Michigan State University*

This paper presents a high-speed, high-resolution, and low-power CMOS switched-current cyclic Analog-to-digital converter (ADC). The high performance is attributed to the use of the following components: (1) a high-performance residual amplifier which takes two clock cycles to double a current; and (2) an efficient Cyclic RSD algorithm which provides 1.5b resolution without using two matched reference currents. Simulation results show that the developed ADC achieves 12-bit resolution, a conversion rate of 100ns per bit, and a power consumption of 1.9mW, where the low-cost MOSIS SCAN20 2um CMOS process and 3.3V supply voltage are employed.

TPA15 – Sensors and Related Circuits Poster Session

Chair: Richard Colbeth

Varian Imaging Products

Chair: Igor M. Filanovsky

University of Alberta

2:00pm – 3:30pm - ***Room: Serra Ballroom Back III***

*3:30 pm – 4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

TPA15-1-- CMOS 1D and 2D N-Well Tetra-Lateral Position Sensitive Detectors

Chowdhury, Mohamed Foysol, *University of Kent at Canterbury*

In this paper characteristics of one dimensional (1D) and two dimensional (2D) N-well tetra-lateral Position Sensitive Detectors (PSD) structures are reported. The PSDs have been fabricated using standard CMOS process. Measurements of the device parameters (dark current, resistance, and junction capacitance), responsivity, position resolution, position linearity and variations due to optical spot size shows that such PSD structures exhibits unique characteristics that are worth considering when designing the biasing and linearization circuits. Overall observation shows that both PSD structures can be successfully fabricated using standard CMOS technology. These measurements were primarily taken to determine the range of operating conditions for each device. This information is intended for chip designers to deduce specifications for designing on-chip signal conditioning and signal processing circuits to improve the performance of the device. Applications of PSDs include optical lateral, rotational or angular position sensing, surface smoothness measurements, range-finding instrumentation, 3D imaging and micro-mechanics.

TPA15-2-- High Performance CMOS Position-Sensitive Photodetectors (PSDs)

Mäkynen, Anssi Jaakko, *University of Oulu*

Five different constructions of optical position-sensitive detectors (PSDs) implemented using standard CMOS technology are reported. The results show that CMOS technology provides means for implementing high performance PSDs.

TPA15-3 -- Measuring Temperature Calibration Free with Bipolar Transistors

Kanoun, Olfa, *Universität der Bundeswehr München*

The use of pn-junctions for temperature measurement has gone through several stages from the simple temperature sensor to the integrated sensor. In this paper we introduce the use of bipolar transistors for a calibration free temperature measurement. The elimination of the need to calibrate enables to reduce the production and maintenance costs of sensors.
Not all known temperature measurement methods using bipolar transistors are able to realize a calibration free temperature measurement. Even methods realizing a calibration free temperature measurement like the well-known method by Verster have been used in practice with calibration in order to realize an acceptable accuracy. We propose to use an accurate i-u characteristic model and to take more measured i-u points into account. This improves the accuracy of measurement without affecting the calibration free behaviour.

TPA15-4 -- Two Temperature Sensors Realized in BiCMOS Technology

Filanovsky, Igor M., University of Alberta

Two temperature sensors realized in BiCMOS technology are described. The first sensor is using, as a temperature sensitive element, a circuit of the threshold extractor. The output of this circuit provides the p-cannel transistor threshold voltage that linearly changes with temperature. The second sensor is using a bridge that includes polysilicon and base-diffused resistors. A one-stage operational amplifier amplifies the output voltage of the sensors. The temperature siulation of the sensor circuits shows that the circuit with extractor has a more linear temperature characteristics than the circuit with the bridge.

TPA15-5 -- A CMOS Integrated Infrared Radiation Detector for Flame Monitoring

Malcovati, Piero; Maloberti, Franco; and Poletti, Matteo, *University of Pavia* and Francesconi, Fabrizio, *Micronova Sistemi S.r.l.*
Bendiscioli, Paolo and Valacca, Roberto, *University of Pavia*

This paper presents an integrated infrared radiation detector for flame monitoring applications, fabricated in CMOS technology. The system discriminates the radiation of the flickering flame in an oil burner from the steady background radiation generated by the furnace by considering only the harmonic components of the infrared signal in the band from 50 Hz to 250 Hz. In order to maximize the flexibility and the robustness of

the system, most of the signal processing is performed in the digital domain. Experimental results on an integrated prototype, confirming the validity of the proposed approach, are reported.

TPA15-6 -- A Multi-mode X-ray Imager for Medical and Industrial Applications

Colbeth, Richard E., *Varian Imaging Products*

This paper describes a multi-mode, digital imager for real-time x-ray applications. The imager has three modes of operation: low dose fluoroscopy, zoom fluoroscopy, and high resolution radiography. These modes trade-off resolution or field-of-view for frame rate and additionally optimize the sensitivity of the imager to match the x-ray dose used in each mode. This large area sensing technology has a form factor similar to that of an x-ray film cassette, no geometric image distortion, no sensitivity to magnetic fields, a very large dynamic range which eliminates repeat shots due to over or under exposure, 12 bit digital output and the ability to switch between operating modes in real-time. Medical applications include fluoroscopy and radiography, while non-destructive test (NDT) applications might include solder joint verification on printed circuit boards and parts inspection in the automotive and aerospace industries.

TPA15-7 -- Novel Low Power Class-B Output Buffer

Yu, Pang-Cheng and Wu, Jiin-Chuan, *National Chiao-Tung University*

*This paper describes the design of a Class-B output buffer for driving large capacitance load in flat panel display. Due to the large number of output buffers on a column driver chip, the quiescent current of the output buffer must be reduced. A comparator which produces full swing output is used in the negative feedback path to eliminate quiescent current in the last stage. The proposed circuit was implemented in a 0.8mum CMOS process. The measured maximum static current is 54muA. With 5V supply voltage and 600pF load, the tracking error voltage is less than +/-8mV and the output swing is from 0.5V to 5V. The settling time for 4V swing to 0.2% is 8mus, which is more than adequate for driving 1204*1280 pixels LCD panel with 86Hz frame rate.*

TPA15-8 -- A Novel Image Sensor with Flexible Sampling Control

Ohtsuka, Yasuhiro; Hamamoto, Takayuki; Aizawa,Kiyoharu, and Hatori,Mitsutoshi, *University of Tokyo*

We propose a new sampling control system on image sensor. Contrary to the random access pixels, the proposed sensor is able to read out spatially variant pixels at high speed, without inputting pixel address for each access. The sampling positions can be changed dynamically by rewriting the sampling position memory. Since the proposed sensor has sampling position memory that stores the sampling control order, it is able to easily control sampling position. We can achieve any spatially varying sampling patterns.

TPA15-9 -- A 128x128 Imaging Array Using Lateral Bipolar Phototransistors in a Standard CMOS Process

Sandage, Robert, W., *Georgia Institute of Technology*

A 128x128 element photodetector array has been fabricated using lateral bipolar phototransistors in a standard 1.2 um digital CMOS process. One-bit image processing for the array is accomplished through the use of a current mode comparator. Images focused on to the photodetector array have been successfully captured and are presented in this paper.

TPA15-10 --Single Chip CMOS Image Sensors for a Retina Implant System

Schwarz, M.; Hauschild, R.; Hosticka, B.J.; Huppertz, J.; Kneip, T.; Kolnsberh, S.; Mokwa, W., and Trieu, H.K., *Fraunhofer Institute of Microeletronic Circuits and Systems*

This work describes the architecture and realization of microelectronic components for a retina implant system that will provide visual sensations to patients with photoreceptor degeneration by applying electrostimulation of the intact retinal ganglion cell layer. Special circuitry has been developed for a fast single-chip CMOS image sensor system which provides high dynamic range of more than seven decades (without mechanical shutter) corresponding to the performance of the human eye. This image sensor system is directly attachable to a digital filter and a signal processor that compute the so -called receptive-field function for generation of the stimulation data. These external components are wireless linked to an implanted flexible silicon multielectrode stimulator which generates electrical signals for electrostimulation of the intact ganglion cells. All components, including additional hardware for digital signal processing and wireless data and power transmission have been developed for fabrication using our in-house standard CMOS-technology.
Systems

TPA15-11 --An Analog VLSI Velocity Sensor Using the Gradient Method

Deutschmann, Rainer Alexander, *Walter Schottky Institut*; and Koch, Christof, *California Institute of Technology*

Smart vision sensors that unify imaging and computation on one single chip offer great advantage over conventional sensor systems, where the computational part is usually performed separately and serially on a digital computer. Using parallel analog VLSI design principles, compact, low power, inexpensive and real time sensors can be built even in standard CMOS processes. In this paper we present the first working analog VLSI implementation of a 1-D velocity sensor that uses the gradient method for spatially resolved velocity computation. We use a novel floating gate wide linear range amplifier and a floating gate division circuit. The division by zero problem of the gradient method has been solved. The sensor velocity output linearly codes the stimulus velocity over a wide range, is independent of contrast down to 20 percent contrast and indicates the correct direction-of-motion down to 4 percent contrast. In a circular pixel arrangement the sensor reports the rotational velocity up to 350 rpm.

TPA15-12 -- A Single Fourier Series Technique For The Simulation And Analysis Of Asynchronous

Pulse Width Modulation In Motor Drive Systems

Guinee, Richard Anthony, *Cork Institute Of Technology*; and Lyden, C., *NMRC University College*

A generalized single Fourier series description is presented for the simulation and analysis of asynchronous pulsewidth modulation (PWM) in brushless motor drive (BLMD) systems. This simple expedient eliminates the need for very small time steps in resolving the PWM waveform edge transition times, within a switching interval, without loss of simulation accuracy. Graphed simulation data indistinguishable from that for analog comparator circuit implementation is presented for three forms of PWM based on the generalized Fourier series representation. Substantial savings of up to fifty fold in motor drive simulation time are achieved without impairment to simulation accuracy.

PANEL DISCUSSION

TPB1 – Government Funded Research

4:00pm – 5:30pm - ***Room: Serra Ballroom II***

PANEL DISCUSSION

TPB2 – Teaching Circuits, Systems, Electronics and Signal Processing in the 21st Century

4:00pm – 5:30pm - ***Room: Steinbeck Forum***

TPB2-1 -- Analog Signal Processing: A Better Way to Teach

Munson Jr., David C., and Jones, Douglas L., *University of Illinois*

A new undergraduate curriculum in electrical engineering has been adopted by the Department of Electrical and Computer Engineering at the University of Illinois. The most radical change has been the introduction of ECE 210, Analog Signal Processing, in place of both the sophomore-level circuit analysis course and the junior-level signals and systems course. The new course combines core material from these traditional courses, along with applications such as AM radio and a modest laboratory component, in a way that improves both the students' understanding and their motivation. The new course still serves well as the core of the required curriculum and as a prerequisite for subsequent courses, while realizing a two-credit-hour saving in the early curriculum and allowing more time for advanced signal processing and systems courses in future semesters.

TPB2-2 --Teaching Circuits and Electronics to First-Year Students

Tsividis, Yannis, *Columbia University*

This paper discusses the philosophy, implementation, and results of an experimental course in circuits and electronics, which is offered to first-year students at Columbia University. The course includes a strong laboratory component. The results, which are reported, have been excellent.

TPB2-3 -- Teaching, Circuits, Systems, and Signal Processing

Diniz, Paulo S. R., *Federal University of Rio de Janeiro*

This paper presents some critical analysis of the current trends in teaching circuits, systems and signal processing. It has been widely discussed throughout the world how deep should circuits be taught to Electrical and Computer Engineers and how important is this knowledge to the engineer career. Another common debate is how and when should circuits, systems and signal processing be taught in future curricula. These issues are difficult to address, however open debates can shed new light and lead to creative solutions. In this paper a strategy to teach circuits, systems and signal processing is discussed.

TPB2-4 -- Introductory Circuits: A Course in Crisis

Davis, Artice M., *San Jose State University*

This paper presents an analysis of the problems the introductory circuits course is facing, including a critique of the students taking the course and the texts available, and offers some suggestions for solutions to these problems.

Plenary Wednesday

8:05am – 8:45am (Serra Grand Ballroom)

Dr. Greg Papadopoulos, Vice President, Chief Technology Officer, Sun Microsystems, Inc.

Title: Billions and Billions of Devices Served: Fundamental Challenges for the Network Age

WAA1 – Adaptive Signal Processing III

Chair: A. Antoniou

University of Victoria

9:00am – 12:30pm - ***Room: Colton I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA1-1 -- DOA Estimation of Speech Source with Microphone Arrays

Jian, Ming, *Nanyang Technological University*

In this paper, we address the problem of DOA estimation for speech signal with a linear equal space microphone array. Based on the speech signal spectrum, a frequency selective wideband DOA method is proposed without a priori knowledge about the source location. Resampling, spatial interpolation and least square technique are employed in the proposed DOA estimation for the far field and near field cases. Computer simulations results show that the proposed method can be used to estimate the DOA of the speech signal at a low signal to noise ratio and with strong interferences and reverberations.

WAA1-2 -- Two New Model Order Selection Approaches for ARMA System Modeling Using the Two-Dimensional Frequency Domain Least Square Algorithm

Mikhael, Wasfy B., *University of Central Florida;* Roman, Jaime R., *Scientific Studies Corporation;* Zhang, Qingwen, *University of Central Florida;* and Davis, Dennis, *Scientific Studies Corporation*

The linear algorithm for two-dimensional least square approximation in the frequency domain (2D-FD-LS) is well-established and has been applied successfully to 2D signal representation and image noise cancellation. But it does not give any explicit model order selection method. In this paper, two approaches for model order selection for the 2D-FD-LS algorithm are proposed. One is a rank-checking method, and the other is a grouping measure based method. Analysis and simulation results demonstrate the applicability of these new approaches. The first approach is recommended for deterministic (known spectrum) applications, while the second approach is more suitable for the random case.

WAA1-3 -- An Algorithm-Based Fault Tolerant Method for the 2-D LMS Algorithm

Schmitz, Christopher Dale, and Jenkins, W. Kenneth, *University of Illinois at Urbana-Champaign*

An algorithm-based fault tolerant method termed the fault tolerant least-mean-squares (FTLMS) algorithm is extended from 1-D to 2-D. The algorithm enables the LMS to correct for a particular type of weight update failure called a stuck-at fault. The key to the algorithm is an overcomplete set of vectors used to transform the input. In developing the 2-D version, the properties of performance-enhancing transforms are investigated, leading to a transform structure that gives the algorithm a more desirable convergence rate. Various transforms are evaluated according to their reduction in eigenvalue ratio (EVR) for stationary inputs.

WAA1-4 -- An Adaptive Kalman Filter for the Enhancement of Noisy AR Signals

Doblinger, Gerhard, *Vienna University of Technology*

In this paper, we describe a new adaptive system for the enhancement o fautoregressive (AR) signals which are disturbed by additive broadband noise. The system is comprised of an adaptive Kalman filter operating as a fixed-lag smoother and a subsystem for AR parameter estimation. As opposed to the conventional approach of employing an extended Kalman filter, we estimate the Kalman filter parameters using the enhanced signal and thus establishing a feedback between the Kalman filter output and the estimated parameters. Our system is capable of tracking short-time stationary signals. It is computationally efficient and can easily be implemented on today's integrated digital signal processors.

WAA1-5 -- Acceleration of Normalized Adaptive Filtering Data-Reusing Methods using the Tchebyshev and Conjugate Gradient Methods

Soni, Robert A., and Jenkins, W. Kenneth *University of Illinois at Urbana-Champaign;* and Gallivan, Kyle A., *Florida State University*

New normalized data reusing can significantly improve convergence rates over traditional LMS adaptive filtering methods. However, these methods can still be slow to converge for highly-correlated input data. The convergence rate of this normalized adaptive algorithm can be significantly improved by accelerating these methods using conjugate gradient and Tchebyshev algorithms. Use of these acceleration techniques can be shown to be approximately equivalent to the popular methods of affine projection albeit at a lower overall computational complexity. Simulation examples illustrate that significant improvement may be obtained using thse methods of accleration. Theoretically, optimal performance bounds for this method of data reusing are illustrated by proof and simulation.

WAA1-6 -- An Adaptive Beamspace Algorithm for Mobile Satellite Communications Systems using Orthogonal Waveforms and Convolutional Codes

Terry John D. and Williams, Douglas B., *Georgia Institute of Technology*

In this paper, a novel adaptive beamspace algorithm is presented for mobile satellite communications. It is shown that convolutional codes combined with orthogonal waveforms over the complex field provide both co-channel interference mitigation and reduced order computations for a multi-beam antenna. Reduced computational complexity is achieved by selecting a subset of the fixed beams based on a threshold computed from estimates of the bit error rates (BER) at the outputs of each of the beams. The subset of beams is subsequently used to perform adaptive beamspace processing to reduce the co-channel interference. Finally, the performance of the algorithm is evaluated via computer simulations for both fading and non-fading channels in the presence of co-channel interference.

WAA1-7 -- On Unbiased Adaptive IIR Filtering Algorithms

Cousseau, Juan E., and Don~ate, Pedro D., *Universidad Nacional del Sur;*and Diniz, Paulo S. *Universidade Federal do Rio de Janeiro*

Some properties of a recently proposed unbiased criteria for adaptive IIR filtering, namely the Master-slave Expanded Numerator Algorithm (XNA), is investigated. The XNA algorithm combines the minimization of two criteria that are quadratic in the parameters. Although the XNA method achieves an unbiased behavior in sufficient-order system identification applications, it generates undesired stationary points. Through the study presented in this paper, explicit expressions for the unwanted stationary points can be obtained. By closely examining the obtained results, a new unbiased adaptive IIR filtering algorithm is presented. Using similar ideas to the Steiglitz-McBride method, the new algorithm is based on the minimization of an off-line error function After the proposal of the new unbiased (off-line) algorithm, which is quadratic in the parameters, we present the analysis of the possible stationary points. Some examples are shown illustrating the performance of the new algorithm in a system identification application.

WAA1-8 -- A Context Based Lossless Compression Algorithm for Ionogram Data

Ye, Hua, *La Trobe University*

Context modeling has recently drawn much research interest to improve the performance of a compression algorithm for binary data such as images. This is because it can help to remove the remaining statistical redundancy among the data after the prediction stage. In this paper, a simple context modeling scheme is proposed in the lossless compression of ionogram data. Experiments show that compared with the one without context modelling, this scheme can provide an over 13% increase in the average compression ratio for the sample data files with almost nothing added in the computation complexity.

WAA2 – Steerable Filters and Applications — Special Session

Chair: Vedat Tavsanoglu

Southbank University

9:00am – 12:30pm - ***Room: Colton II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA2-1 -- Steerable Pyramid Filters for Selective Image Enhancement Applications

Wu, Qiang, and Castleman, Kenneth R., *Perceptive Scientific Instruments, Inc.*

In this paper we describe a method we developed for selective detection and enhancement of image feature patterns. A set of directional basis filters were designed to detect the image features of interest, and a steerable pyramid transform [1,2] is used to generate a multiscale representation of the image features that has desirable shift and rotation invariance. By analyzing and selectively processing the transform coefficients, image feature detection and enhancement can be achieved with designed flexibility in scale, orientation, location, and degree of enhancement. Unlike traditional

techniques, this new method promises the selectivity and flexibility desirable in many image enhancement applications. Preliminary experimental results are presented to exemplify the feasibility of the approach.

WAA2-2 -- Simplified Design of Steerable Pyramid Filters

Castleman, Kenneth R., *Perceptive Scientific Instruments, Inc.*

The steerable pyramid decomposition is an invertible representation similar to the two-dimensional discrete wavelet transform, but with interesting shift- and rotation-invariance properties. It is slightly overcomplete and amenable to a filter bank implementation via convolution and down- and up-sampling operations. This paper presents a simple method for designing the FIR filter kernels required to implement the transform.

WAA2-3 -- Multirate Separable Implementation of Steerable Filter Banks

Manduchi, Roberto, *Caltech*

This paper describes efficient schemes for the computation of a large number of differentially scaled/oriented filtered versions of an image. Previous work has generalized the well-known steerable/scalable ("deformable") filterbank structure by imposing X-Y separability on the basis filters. This systems, designed by an iterative projections technique, was shown to achieve substantial reduction of the computational cost. To reduce the memory requirement, we adopt a multirate implementation. The resulting structure, however, is not shift-invariant - it gives raise to "aliasing". We introduce a design criterion for multirate deformable structures that jointly controls the approximation error and the shift-variance.

WAA2-4 -- A Common Framework for Steerability, Motion Estimation, and Invariant Feature Detection

Teo, Patrick C., *Stanford University;* and Hel-Or, Yacov, Hewlett-Packard Labs, Israel

Many problems in computer vision and pattern recognition involve groups of transformations. In particular, motion estimation, steerable filter design and invariant feature detection are often formulated with respect to a particular transformation group. Traditionally, these problems have been investigated independently. From a theoretical point of view, however, the issues they address are related. In this paper, we examine the relationships between these problems and propose a theoretical framework within which they can be discussed in concert. This framework is based on constructing a natural representation of the image for a given transformation group. Within this framework, many existing techniques of motion estimation, steerable filter design and invariant feature detection appear as special cases. Furthermore, several new results are direct consequences of this framework.

WAA2-5 -- Handwritten Character Recognition Using Steerable Filters and Neural Networks

Tufan, Emir *Istanbul University*

This paper proposes a new approach for handwritten character recognition, using steerable filters and neuarl networks. Based on a training set of 50 unknown handwritten digits, 90% correct with less than 1% wrong recognition is provided.

WAA2-6 -- Motion Analysis Using Steerable Filters for the Application to Low Quality Images

Tavsanoglu, Vedat, *Southbank University;* Buhmann, Sitta, *Hochschule Bremen*

In this paper we present a method for the analysis of motion that is applicable to low quality images. The method uses two-dimensional steerable filters for orientation analysis and computes velocity fields out of the orientation information. We introduce a projection method that allows to use the two-dimensional filters instead of three-dimensional filtering. In addition this projection method is a very powerful tool for the restoration of motion information out of very low quality images.

WAA2-7 -- The SVD Approach for Steerable Filter Design

Herpers, Rainer, and Sommer, Gerald, *University of Kiel; and* Michaelis, Markus, *Plettac Electronics*

The first processing step in computational early vision usually consists of convolutions with a number of kernels. These kernels often are derived from a mother kernel that is rotated, scaled, or deformed with respect to other degrees of freedom. This paper presents an efficient computational approach to calculate the responses of arbitrary mother kernels with arbitrary deformations. Analytical solutions to this problem in most cases are difficult or not possible. Therefore, we present in this paper a numerical approach that emphasizes an algebraical point of view.

WAA3 – Networks for Biological Computing & Fuzzy Logic

Chair: Lex A. Akers

University of Texas at San Antonio

9:00am – 12:30pm - ***Room: Colton III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA3-1 -- An Adaptive Front End for Olfaction

Apsel, Alyssa, *The John Hopkins University*; Stanford, Theron, *California Institute of Technology* and Hasler, Paul, *Georgia Institute of Technology*

We have developed a high-resolution front-end chemical sensing system with time adaptation. This circuit uses analog subthreshold floating-gate technology to produce normalized percent change outputs over a wide range of sensor resistances. We fabricated these circuits in a standard CMOS 2mm process. We present the analytical and experimental results of this system.

WAA3-2 -- Adaptation in an AVLSI Model of a Neuron

Simoni, Mario; and DeWeerth, Stephen P., *Georgia Institute of Technology*

We have designed, fabricated, and tested an analog Very Large Scale Integrated (aVLSI) circuit model of a neuron that facilitates self-adaptation of its parameters. This self-adaptation results from a negative feedback loop that modulates conductances based on the activity of the "cell" as described in [1]. We show that the addition of this self-adaptation to our model neuron can facilitate: 1) single parameter control over a multi-parameter system; 2) stability of the system to fluctuations in parameters; 3) coordinated modulation of parameters to achieve a desired behavior.

WAA3-3 -- Biologically-Motivated Neural Learning in Situated Systems

Damper, Robert Ivan, *University of Southampton*; and Scutti, T.W., *University of Nottingham*

We describe the autonomous robot ARBIB. This uses biologically-motivated forms of learning to adapt to its environment. ARBIB's `nervous system' has a non-homogeneous population of spiking neurons, and uses both non-associative and associative forms of learning to modify pre-existing (`hard-wired') reflexes. As a result of interaction with its environment, interesting and `intelligent' light-seeking and collision-avoidance behaviors emerge which were not pre-programmed into the robot (or `animat'). These behaviors are similar to those described by other workers who have generally used behaviorally-motivated reinforcement learning rather than biologically-based associative learning. The complexity of observed behavior is remarkable given the extreme simplicity of ARBIB's `nervous system', having just 33 neurons. We take this to indicate that great potential exists to explore further ``the animat path to AI''.

WAA3-4 -- FWNN for Interval Estimation with Interval Learning Algorithm

Jiao, Licheng; Liu, F.; and Wang, L., *Xidian University*

In this paper, a wavelet-based fuzzy neural network for interval estimation of processed data with its interval learning algorithm is proposed. It is also proved to be an efficient approach to calculate the wavelet coefficient.

WAA3-5 -- FDSP: A VLSI Core for Adaptive Fuzzy and Digital Signal Processing Applications

Sultan, Labib, *Microfuzz Technologies Inc*

The FDSP (Fuzzy Digital Signal Processor) is a new device that combines fuzzy and DSP in a single core well adapted to be hosted by low cost microcontrollers. The FDSP offers economic solution to implement adaptive fuzzy digital signal processing. The fuzzy acts as a controller or an adaptive element to a DSP system to implement adaptive filters, noise cancellers, estimators, channel equalizers, etc. We demonstrate the use of the FDSP to implement Hard Disk Drive controller that combines quazi-optimum seek-track control, adaptive noise filters, and velocity estimator, Other applications of the FDSP include non-linear Imaging filters and motion estimators and other systems for multimedia processing.

WAA3-6 -- A Current-Mode Piecewise-Linear Function Approximation Circuit Based on Fuzzy-Logic

Manaresi, Nicolo'; Rovatti, Riccardo; Franchi, Eleonora; and Baccarani, Giorgio, *D.E.I.S. - University of Bologna*

An analog circuit for function approximation working in current-mode is described. It implements a piecewise-linear fuzzy system: the membership functions are generated by the daisy-chain connection of identical blocks, resulting in a grid placement of the rules, and programming is achieved by binary encoded digital words representing the consequents of the rules. An approximated analytical model is derived, relating the I/O spread with the bias current variation. The current level

allows speed and precision to be traded off for power consumption, while maintaining the same normalized I/O characteristic. The circuit is shown to operate correctly both in strong and weak inversion, with a bias current varying by two orders of magnitude.

WAA3-7 -- Embedded Fuzzy Control on Monolithic DC/DC Converters

Criscione, M., *SGS-THOMSON Microelectronics;* Lionetto, A., and Nunnari, G., *University of Cantania;*and Occhipinti, L., *SGS-THOMSON Microelectronic*

Several fuzzy control applications have been proposed for nonlinear control of nonlinear power supply devices. Some control problem in fact will arise in DC/DC converters due to their intrinsic nonlinear nature and in some case, of unstabilities and tendency to oscillate, lying with some particular topologies. The work presented reports a monolithic approach implementing an embedded fuzzy controller within classical DC/DC converter boost topology, with current-mode direct PWM control. It will be demonstrated, as well, how the proposed approach will solve the intrinsic unstability of such topology, when acting under continuous operating mode. Finally the IC implementation will be briefly introduced, referring to ST mixed technology.

WAA3-8 -- A Wavelet-Based Fuzzy Neural Network for Interpolation of Fuzzy If-Then Rules

Jiao, Licheng, *Xidian University*

In this paper, a wavelet-based fuzzy neural network with its structure and learning algorithm is proposed and the simulation results are given to prove its feasibility.

WAA4 – Image and Video Processing III

Chair: Peter Pirsch

University of Hannover

9:00am – 12:30pm - ***Room: Ferrante I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA4-1 -- A Comparative Study of DCT and Wavelet Based Coding

Xiong, Zixiang; *University of Hawaii*; Ramchandran, Kannan, *Princeton University*; Orchard, Michael T., *University of Illinios at Urbana-Champagne*; and Zhang, Ya-Qin, *Sarnoff Corporation*

We study the performance difference of the discrete cosine transform(DCT) and the wavelet transform for both image and video coding, while comparing other aspects of the coding system on an equal footing .Based on the state-of-the-art coding techniques, we point out that, for still images, wavelet outperforms DCT with a coding gain of about one dB in PSNR. For video coding, the advantage of wavelet schemes is less obvious. We believe that image and video compression algorithm should be addressed from the overall system viewpoint. Quantization, entropy coding, and paying attentions to details are more important than spending all the efforts on optimizing the transform.

WAA4-2 -- A Two-Layer MPEG2-Compatible Video Coding Technique Using Wavelets

Zan, Jinwen; Zhu, Wei-Ping; Ahmad, M. Omair, and Swamy, M.N.S., *Concordia University*

In this paper, a two-layer hierarchical video coding technique that is compatible with MPEG2 is presented. By using a simplified version of the Mallat algorithm [1], a video signal is decomposed as two constituent signals, the smoothed signal comprising low-frequency content and the edge part representing the high-frequency information. The smoothed signal is then encoded into an MPEG2 video stream, while the edge information is encoded by utilizing the chain code [6] into an MPEG2 private stream. By applying this coding strategy, the artifacts such as the blocking effect that is usually present in conventional block-based coding schemes, especially at low bit rate, and the ringing effect which may occur in a wavelets-based method, are both overcome. Simulation results show that the proposed coding schemeis capable of producing high-quality reconstructed video signals.

WAA4-3 -- An Adaptive Video Sub-Sampling Technique for the Conversion between High and Low Resolution

Wong, Peter H.W.; Au, Oscar C.; Wong, Justy W.C.; and Tourapis, A., *Hong Kong University of Science and Technology*

An adaptive sub-sampling technique is proposed for the conversion of high-resolution video to low-resolution video, which will eventually be converted back to high resolution. This technique can preserve high spatial frequency information by exploiting the temporal correlation of stationary regions without any extra storage or transmission bandwidth. Coding complexity can be reduced by a factor of four if the video is to be eventually displayed in high-resolution, with small degradation in visual quality and peak-signal-to-noise ratio. Most of the edge information can be preserved

when the low-resolution video is converted back to high-resolution video and significant improvement can be obtained compared with conventional methods.

WAA4-4 -- Computation Reduction for Discrete Cosine Transform

Pao, I-Ming and Sun, Ming-Ting, *University of Washington*

This paper presents a method to accelerate software video encoders by reducing the number of operations for Discrete Cosine Transform (DCT) and quantization. We present a model of DCT coefficients based on the information of motion compensated difference blocks. The relationship between the quantization level and DCT coefficients is also studied. Based on the model, we can adaptively make the decision of DCT calculations. A fast algorithm is also proposed for approximating the 4x4 low-frequency coefficients. The results show that significant computation reductions can be achieved with negligible peak signal-to-noise ratio (PSNR) degradations.

WAA4-5 -- Scalable Coding of Video Objects

Haridasan, Radhakrishnan and Barns, John S., *University of Maryland*

This paper provides a methodology to encode video objects in a scalable manner with regard to both content and quality. Content scalability and quality scalability have been identified as required features in order to support video coding across different environments. Following the object-based approach to coding video, we extend our previous work on motion-based segmentation by using a time recursive approach to segmenting image sequences and decomposing a video "shot" into its constituent objects. Our formulation of the segmentation problem enables us to design a codec in which the information (shape, texture and motion) pertaining to each video object is encoded independent of the other. The multiresolution wavelet decomposition used in encoding texture information is shown to be helpful in providing spatial scalability. Our codec design is also shown to be temporally scalable.

WAA4-6 -- Hybrid DCT/Wavelet I-frame Coding for Efficient H.263+Rate Control at Low Bit Rates

Song, Hwangjun; Kim, Jongwon; and Kuo, C.-C. Jay, *University of Southern California*

At low bit rates, the bit budget for I-frame coding in H.263+ can be too high to be practical. A hybrid DCT/wavelet transform based I-frame coding is proposed in this work as a solution to the rate control problem. This new coder is compatible with the H.263+ bit stream syntax, and aims at an R-D optimized performance with a reasonable amount of computational complexity. By employing fast estimation of the coding efficiency with a rate-distortion model andperforming an R-D based rate allocation, the hybrid coding scheme achieves higher coding gain at low bit rates.

WAA4-7 -- Hybrid Search Algorithm for Block Motion Estimation

Cheung Chok-Kwan and Po, Lai-Man, *City University of Hong Kong*

An hybrid block matching algorithm for motion estimation is proposed in this paper. In this algorithm, a motion block is classified as either large or small motion by making use of the correlation between the block distortion measure of the origin checking point and the magnitude of the motion vector. According to the classified motion type, one of the two fast block matching algorithms --- the four-step search and block-based gradient descent search, is employed for the motion estimation. An adaptively updated threshold is used for the motion type classification. Experimental results show that the proposed algorithm can achieve better MSE performance than the two algorithms due to the increased chance for the individual algorithm to search its favorite motion type.

WAA4-8 -- Low-Power MPEG2 Encoder Architecture for Digital CMOS Camera

Hsieh, Jeff Yeu-Farn and Meng, Teresa H., *Stanford University*

A low-power, large-scale parallel MPEG2 encoder architecture for a single-chip digital CMOS video camera is discussed in this paper. This single-chip architecture includes a 640x480 array of CMOS photo diodes, each pixel with an 8-bit dynamic range per color plane, and embedded DRAM for storing 4 frames of data. The parallel processor architecture is designed to implement highly computationally intensive image and video processing tasks such as color conversion, DCT, and motion estimation for MPEG2. When clocked at 40 MHz with two ALU pipeline stages, it delivers a processing performance of 1.6 billion operations per second (BOPS) and can support frame rates of up to 30 fps. The architecture is specifically designed for low power consumption. When implemented in a 0.2 micron CMOS technology at a 1.5 V supply voltage, it will consume 40 mW, thus providing a power efficiency of 40 BOPS/Watt.

– Wireless/Mobile Communications

Chair: Donald Gingras

SPAWAR Systems Center

9:00am – 12:30pm - ***Room: Ferrante II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA5-1 -- A Priority-Based Random Access Spread-Spectrum Protocol for Integrated Voice/Data Packet Networks

Gingras, Donald F. and Lapic, Stephan K., *SPAWAR Systems Center*

In this paper we propose and evaluate a multiple access protocol for synchronous cellular packet direct-sequence code-division multiple access (DS-CDMA) networks. Most CDMA systems assign a unique spreading code to each terminal, here a joint TDMA/CDMA protocol, which allows all terminals to share a group of spreading codes, is presented. Two service classes are provided; a best-effort "datagram" service with priority queues and a guaranteed bandwidth circuit service. The performance of the protocol is evaluated via simulation. Two performance measures are used to assess the protocol; voice packet dropping probability and data packet delay.

WAA5-2 -- A Chip-Interleaving DS SS System and Its Performance Under On-Off Wide-Band Jamming

Gui, Xiang and Ng, Tung Sang, *The University of Hong Kong*

A modified direct sequence spread spectrum system employing the concept of chip-interleaving is proposed. Its performance under periodic on-off wide-band jamming is analyzed and closed-form bit error rate (BER) performances of the proposed system for both the best case and the worst case are obtained. The proposed system is compared with conventional system using numerical examples.

WAA5-3 -- A Genetic-Algorithm-Based Multiuser Detector For Multiple-Access Communications

Wang, Xiao-Feng; Lu, Wu-Sheng; and Antoniou, Andreas, *University of Victoria*

We propose a new detector for multiuser communications, which is based on the maximum-likelihood decision rule and uses a genetic algorithm in conjunction with a modified Viterbi algorithm to detect the user bits sequentially. The major advantage of the proposed detector is that it provides a trade-off between performance and computational complexity. Simulation results show that the proposed detector achieves similar performance to that of two well-known suboptimal linear detectors with a lower computational complexity.

WAA5-4 -- A New Multiple Access Protocol for Multimedia Wireless Networks

Salles, Ronaldo Moreira and Gondim, Paulo Roberto de Lira, *Military Institute of Engineering*

We design and analyze the performance of a new multiple access protocol, designed to attend multimedia traffic in cellular networks and wireless PCS. It is based on slotted-ALOHA and on the permission probability concept, modified in order to allow a different treatment for each kind of traffic. A first variation of the protocol (CPMA: Constant Permission Probabilities Multiple Access) assigns for each kind of traffic a constant and different permission probability value. In a second variation (DPMA: Dynamic Permission Probabilities Multiple Access), we dynamically assign permission probabilities using an extension of the Pseudo-Bayesian Algorithm. These schemes guarantee maximum priority to voice traffic and good channel utilization. Simulation results to voice, low delay data, ATM traffic and high delay data are presented with respect to their QoS requirements. We observe that DPMA presents a better performance when compared to CPMA, due to its adaptability to traffic changes.

WAA5-5 -- A DS-CDMA Receiver Using Exponentially Weighted Despreading Waveforms

Huang, Yuejin and Ng, Tung Sang, *University of Hong Kong*

This paper presents a DS-CDMA receiver using exponentially weighted despreading waveforms (WDW). The chip weighting waveforms are designed for the purpose of multiple access interference (MAI) rejection by emphasizing the transitions of the received signal of interest. The WDW is determined only by one parameter, which leads to easy tuning of the WDW in practice to achieve the best performance. As a result, we show that the proposed receiver can reject MAI without knowing co-user's spreading codes, timing, and phase, and hence increase system capacity. Analysis and numerical results show that the proposed receiver outperforms the conventional receiver especially when MAI is significant. Finally, a discussion on the effect of bandlimited spreading signals is also given on the practical implications of the proposed technique.

WAA5-6 -- Blind Joint Equalization and Multiuser Detection for DS-CDMA in Unknown Correlated Noise

Wang, Xiaodong and Poor, H. Vincent, *Princeton University*

The problem of blind demodulation of multiuser information symbols in a high-rate dispersive CDMA network in the presence of multiple-access interference (MAI), intersymbol interference (MAI) and unknown correlated ambient noise, is considered. It is assumed that the signal is received by two antennas well separated so that the output noise is spatially uncorrelated. Two subspace methods for estimating the dispersive channel response are examined, based respectively on the singular value decomposition (SVD) and the canonical correlation decomposition (CCD) of the cross-correlation matrix of the signals received by the two arrays. A linear MMSE receiver can be constructed once the channel estimate is obtained. Simulation results show that the CCD-based method substantially outperform the SVD-based method.

WAA5-8 -- A Multiple-Access Interference Suppression Technique Employing Orthogonal/Random Spreading Sequences and a Novel Decentralized Receiver for B-CDMA Forward Link Systems in Multipath Channels

Shin, Sung-Hyuk and Voltz, Peter J., *Polytechnic University*

In this paper, we study a multiple-access interference (MAI) suppression technique employing concatenated orthogonal/random spreading sequences and a novel decentralized linear receiver for B-CDMA forward link in multipath fading channels. The proposed receiver treats the MAI as additional noise, while exploiting in an optimal way the homogeneous characteristics of the MAI which is partically suppressed at the despreader of the receiver by utilizing orthogonal sequences. The matched filter RAKE receiver and inverse filter are also considered for comparison. The system performance is evaluated in terms of required bit-energy to effective noise (MAI-plus-AWGN) power spectral density to achieve an acceptable quality of service. We show that employing the concatenated orthogonal/random spreading scheme in the synchronous forward link, the proposed receiver results in better system performance relative to the others and show the impact of the concatenated spreading sequences on the forward link system performance, as compared to the use of the non-concatenated random spreading scheme.

WAA6 – Deep Submicron Digital Circuit Issues

Chair: Nicholas Rumin

McGill University

9:00am – 10:30am - ***Room: Ferrante III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA6-1 -- Performance Criteria for Evluating the Importance of On-Chip Inductance

Ismail, Yehea I. and Friedman, Eby G., *University of Rochester;* and Neves, Jose L., *IBM Microelectronics*

Two figures of merit are presented for determining whether a section of interconnect should be modeled as either an RLC or an RC impedance. The attenuation that a signal undergoes as it propagates a distance equal to the length of the interconnect line is shown to be a useful figure of merit. The second figure of merit considered in this paper is the ratio of the rise time of the input signal at the driver of an interconnect line to the time of flight of the signals across the line. Circuit simulations of an RLC transmission line and a five section RC II circuit are used to quantify and determine the relative accuracy of an RC model. One primary result of this study is evidence demonstrating that a range of interconnect length exists for which inductance effects are negligible despite the length of the section of interconnect.

WAA6-2 -- Interconnect Inductance Effects on Delay and Crosstalks for Long On-Chip Nets with Fast Input Slew Rates

Lee, Mankoo; Hill, Anthony; and Darley, Merrick H., *Texas Instruments*

In this paper, we address the significance of parasitic inductance on designing signal coupling shields and clock tree distributions in terms of input slew rate and interconnect length by using 3D RLC parasitic extraction and Spice simulation for 500 MHz clocks and 0.15 mm process interconnect technology. We report a larger crosstalk deviation under fast input slew rates and a higher clock skew variation due to wiring inductive effect for low resistive long nets which should be considered for future high-speed design. In addition, we propose a feasible one-level interleaved clock shielding scheme with optimized dimensions for a minimal clock skew and compare it to a worst case signal coupling three-level clock shielding scheme.

WAA6-3 -- Linearized Sub-Optimum Method of Long Wire Interconnections with Uniform Wire Driver

Mu, Fenghao; Alvandpour, Atila; and Svensson, Christer, *Linköping University*

A simple analysis is made on the delay for a uniform long wire interconnection with distributed RC property. The optimal widths of wire and transistor are investigated under different constraints. The analysis is based on an improved switch model and Elmore delay model. A linearized relation between wire width and transistor width is suggested. Performance comparison is made between the absolute optimum and the suggested method by plotting the loci of the optimum solutions. Results show that the linearized relation can achieve a sub-optimum solution quite close to the absolute optimum, and it can be used in the delay calculation.

WAA6-4 -- An Interconnect Transient Coupling Induced Noise Susceeptibility for Dynamic Circuits in Deep Submicron CMOS Technology

Lee, Mankoo and Darley, Merrick H., *Texas Instruments*

This paper investigates the susceptibility of Dynamic Logic (DL) noises which are induced during interconnect coupling signal disturbances. We describe transient current/coltage coupling behaviors for a DL noise analysis in terms of far-end crosstalk peak voltage (DVcr) and DL's weak node noise voltage dip (DVdn) as a function of pull down transistor threshold voltage (Vt) and signal input slew rate (S). The worst case interconnect arrays are modeled with accurate parasitic RLC elements extracted by 3D field solver and are connected to either high Vt and/or low Vt pull down transistor

for DL's noise margin simulations. We fully investigate the impacts of driving signal's pull up/down transistor strength, duty cycle, and different operating conditions on transient crosstalk waveforms.

WAA7 – Power Electronics

Chair: Krishna Shenai

University of Illinois at Chicago

9:00am – 10:30am - ***Room: Bonzai I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA7-1 -- An Adaptive Stepwise Quadratic State-Space Modeling Technique for Analysis of Power Electronics Circuits

Tse, K.K.; Chung, Henry S.H.; and Hui, S.Y.R., *City University of Hong Kong*

A new simulation technique for analysis of power electronics circuits is presented. It is based on using the Chebyshev polynomial to derive an adaptive stepwise quadratic state-space model for each piecewise-linear circuit topology, where the state-space equation sets are integrated with modified nodal formulations (MNF). The key feature of this algorithm is to determine an optimum step size for the model to achieve desired accuracy. The switching instants are directly calculated by solving simple quadratic equations. No prior knowledge of the circuit operations is required. The theoretical predictions are verified with the results obtained in the available literature.

WAA7-2 -- An Efficient Method for Calculating Power Flow Solutions and the Closest Bifurcation Point Using Mathematical Programming

Mori, Hiroyuki; and Iizuka, Fumitaka, *Meiji University*

This paper presents an efficient method for calculating the closest bifurcation point and a pair of multiple power flow solutions with mathematical programming. The formulation of the method may be expressed as the minimization problem to evaluate the closest bifurcation point for given initial conditions. Making use of the conditions of a pair of multiple power flow solutions, they are decomposed into the sum of the bifurcation point and the deviation vectors. The solutions is evaluated by mathematical programming so that the closest bifurcation point is evaluated by minimizing the magnitude of the deviation vector to given power system conditions. The proposed method is successfully applied to a sample system.

WAA7-3 -- Computation of State Variable Sensitivities of PWM DC/DC Regulators and its Applications

Wong, Billy K.H. and Chung, Henry S.H., *City University of Hong Kong*

A generalized technique for computation of state variable sensitivities of PWM dc/dc regulators is presented. The methodology not only considers the sensitivities of the state variable variations, but also takes their effects on varying the topology duration into account. A basic sensitivity graph for single topology is firstly derived. It is then propagated to determine the sensitivities of regulators with multiple topologies. Simple mathematical computation and network transformation are required only. The state variable sensitivity matrix is applied to determine the steady-state operating point, using a newly developed dual-loop iteration algorithm and to examine the stability of operation. The algorithm is illustrated with an example of boost regulator. The theoretical predictions are verified with the results obtained from available literature.

WAA7-4 -- Single-Ended Compact MOS-FET Power Inverter with Automatic Frequency Control for Maximinzing RF Output Power Megasonic Transducer at 3 MHz

Mizutani, Yoko; Suzuki, Taiju;Ishikawa, Jun-ich; Ikeda, Hiroaki; Yoshida, Hirofumi; and Shinohara, Shigenobu, *Shizuoka University*

A single-ended compact MOS-FET DC-to-RF power inverter is built to drive a megasonic transducer having an impedance of as low as 5 to 6 ohms or less at 3 MHz. The operating frequency of the MOS-FET DC-to-RF power inverter is automatically set at the resonating frequency of the megasonic transducer using the PLL so that the RF power in the megasonic transducer is maximized. The impedance of the inverter load consisting of an output transformer, a matching capacitor, a coaxial cable, a megasonic transducer, and a current sensor is calculated to determine the frequency control range of the PLL. In accordance with the result of calculation, the performance of the PLL consisting of a phase-frequency comparator, a lowpass filter, and a VCO is determined. The output power of the single-ended compact MOS-FET power inverter was 25 W with a power conversion efficiency of 70%, when the operating frequency was set at the resonating frequency of the megasonic transducer.

WAA8 – Amplifiers II

Chair: Willy Sansen

Katholic University of Leuven

9:00am – 12:30pm - ***Room: Bonzai II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA8-1 -- A 1.2 v CMOS Op-Amp with High Driving Capability

Ferri, Giuseppe, *Universita' di L'Aquila*

In this work, a new low voltage (1.2 V supply) opamp, able to drive loading resistance as low as 500 W, with 2V/ms slew rate and 380 ns settling time, is presented. The low voltage gain is 80 dB for 1 KW and 124 dB for 1 MW load. The gain bandwidth is 2.4 MHz. The power dissipation is 0.268 mW. The circuit, designed in a standard 0.5m technology, has rail-to-tail input and output stages and constant transconductance with the input common mode signal. Its performances have been obtained combining the topologies of a very efficient output stage and of the input and biasing stages of a CMOS integrated OTA, previously developed.

WAA8-2 -- A 3-V RF CMOS Bandpass Amplifier Using An Active Inductor

Thanachayanont, Apinunt, *Imperial College of Science, Technology and Medicine*

This paper presents the design of a 3-V RF CMOS bandpass amplifier using the recently proposed CMOS active inductor [1]. Negative feedback is used with a cascode amplifier to realise a grounded inductance as a frequency selective element and achieve power amplification simultaneously. The proposed bandpass amplifier, which includes an input matching network and an output voltage buffer for a 50-ohm environment, is designed and simulated with a commercial 0.8-micron n-well BiCMOS process using HSPICE. Simulation results of the bandpass amplifier tuned at a centre frequency of 1 GHz with a quality factor of 56 illustrate that a power gain of 23 dB, and a noise figure of 4.3 dB can be achieved with a power dissipation of 57 mW from a single 3 V supply.

WAA8-3 -- A Low Voltage Op-Amp with Constant-Gm Rail-to-Rail Input and High Swing Self-Biasing Super Cascode Output Stage

Asmanis, Georgios, *Rockwell Semiconductor Systems*

Probably the most important building block in a mixed-signal system is the operational amplifier. Power consumption is a critical performance characteristic in fast Op-Amp designs. Low power supplies have become dominant in modern mixed-signal VLSI systems. Unlike CMOS digital modules, which are functionally insensitive to power supply variations, traditional analog cells not only fail to achieve the expected performance characteristics but may also become totally inoperative. This fact, together with the requirement of high density mixed analog-digital VLSI systems, urges the research of new analog architectures capable of achieving high performance characteristics in exceedingly noisy environments, where the presence of digital circuitry is abandon. Therefore, power supply insensitive, self-biasing architectures are highly advantageous, successfully limiting the design, layout and routing effort and guaranteeing the product success.

WAA8-4 -- A Low-Voltage CMOS Rail-to-Rail Class-AB Input/Output OpAmp with Slew-Rate and Settling Enhancement

Lin, Chi-Hung, and Ismail Mohammed, *Ohio State University*

A low-voltage CMOS rail-to-rail OpAmp with high slew-rate and fast-setting is presented. The input stage is composed of the complementary differential pairs, a pair of modified current-mode maximum selecting circuits (Maximum Current Selecting Circuit II) and a class-AB feedback loop circuit. It achieves rail-to-rail operation, constant-gm , high slew-rate and fast-setting. With this OpAmp topology, the design can be easily performed for a side-range of capacitive loads with a large bandwidth-to-power-consumption ratio. With 2mm and 0.5mm technology respectively, the OpAmp has a high DC gain (³84 dB), and has a bandwidth-to-power-consumption ratio of 13.6MHz/mW and 25.8MHz/mW with capacitive loads of 20pF, 86V/ms, 90V/ms slew-rate and 159ns, 36ns settling-time.

WAA8-5 -- A 1.6V 80uW Rail-to-Rail Constant-Gm Bipolar Adaptive Biased Op-Amp Input Stage

Cardarilli, G.C., and Re, M., *University of Rome "Tor Vergata", and* Ferri, G., *University of L'Aquila*

In the design of operational amplifiers, adaptive biasing topologies help to optimise the trade off between speed characteristics and power consumption. In fact, they give an output current dependent on the input differential voltage, minimising the stand-by current. Anyway, all the adaptive biasing solutions presented in literature require an extra quiescent current and, consequently, an additional static power dissipation. In this paper, this problem is overcome by an innovative adaptive biasing topology, which is here proposed and utilized as an application to a traditional constant transconductance rail-to-rail input stage of a low-voltage (1.6V) low-power (80 mW) bipolar operational amplifier.

WAA8-6 -- A High-Drive High-Gain CMOS Current Operational Amplifier

Pennisi, Salvatore, *DEES - University of Catania*

A novel single-input differential-output CMOS current operational amplifier is presented which provides high gain and high drive capability. The amplifier is designed with a 1.2-um CMOS technology, uses a 5V power supply and dissipates a dc power less than 3 mW. Moreover, it exhibits an open-loop gain of 90 dB and a gain-bandwidth of 11 MHz. Thanks to the use of a novel class AB output stage, the proposed amplifier is able to drive a load resistance of 100 ohm with a maximum bipolar output current of about 15 mA, being the quiescent current in the output branch of only 140 uA. Finally, because of its symmetrical topology, the amplifier is also well suited to be arranged in a fully-differential version.

WAA8-7 -- High Accuracy, High Speed Voltage-Follower

Lidgey, John, *Oxford Brooks University*, and Su, Wenjun, *Qualcomm Inc.*

A novel design technique for high-speed, high-accuracy voltage-follower is presented. The design is based on a floating negative-feedback technique which results in the commonly encountered trade-off between speed and accuracy being released. Details of the design principles are explained and a practical design example is described which is shown to exhibit simultaneously very high speed and very high accuracy.

WAA8-8 -- Feedforward Compensation Techniques in the Design of Low Voltage Opamps and OTAs

Setty, Suma, *Ericsson Components*

This paper presents feedforward compensation techniques for low voltage fully differential folded cascode amplifiers and OTAs. Fully differential folded cascode cells have been fabricated and tested with different feedforward configurations in order to demonstrate and compare the usefulness of these techniques for broadbanding the Gain-Bandwidth product for low voltage, low power CMOS amplifiers and for providing high quality low voltage CMOS OTA integrators.

WAA9 – Switched-Capacitor Techniques

Chair: Marcus Helfenstein

Institute for Signal and Information Processing

9:00am – 12:30pm - ***Room: Bonzai III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA9-1 -- Switched-Capacitor Decimation Filter for 0.8 mu CMOS

Petraglia, Antonio, *Federal University of Rio de Janeiro*

This paper presents the design steps considered in the development of an integrated circuit for a switched-capacitor decimation filter. The design consists of dimensioning the operational amplifiers, capacitances and analog switches, using a supply voltage of 5.5 V for a 0.8 mu technology. Also shown are electrical simulations using PSPICE 5.0 considering both typical and worst case conditions for practical application in telecommunication systems, for a sampling rate reduction from 48.20 MHz to 16.07 MHz. The filter dissipates approximately 46mW (including the output buffer) at 5.5 V, and presents a flat frequency response within 0.12 dB from dc to 3.56 MHz.

WAA9-2 -- A Switched-Capacitor N-Path Decimating Filter

Neves, Rui Ferreira, and Franca, Jose E., *Instituto Superior Tecnico*

In this paper we present the first switched-capacitor (SC) circuit implementation of an N-path decimating filter which has the ability to perform frequency downconversion simultaneous with high selectivity filtering while enabling the use of operational amplifiers with relaxed specifications when compared with the tradicional SC N-path filters. The example given is of a 4-path system using high-pass decimating filters with input and output sampling frequency of 40 MHz and 13.3 MHz, respectively, yielding an overall input sampling frequency of 160 MHz and thus extended input baseband from 0 to 80 MHz. The detailed simulation analysis of the circuit illustrates the resulting frequency downconversion from 60 MHz to 6.6 MHz as well as the effect of various sources of errors, e. g., operational amplifier offset and gain errors, capacitance mismatch and clock skew, in the overall baseband response and image rejection performance.

WAA9-3 -- CMOS Switched-Opamp Based Sample-and-Hold Circuit

Harjani, Ramesh, and Dai, Liang, *University of Minnesota*

This paper presents a sample-and-hold design that is based on a switched-opamp. By using a switched-opamp topology charge injection errors are greatly reduced by turning off the transistors in saturation instead of triode region. A pseudo-differential topology is used to cancel the remaining signal independent clock feedthrough error. Switched opamps with differential pairs in both weak inversion and strong inversion are designed.

Detailed simulation and measurement results of a switched-opamp based sample and hold circuit is used to show its performance superiority over traditional switched capacitor topologies.

WAA9-4 -- Companding Switched Capacitor Filters

Krishnapura, Nagendra, and Tsividis, Yannis, *Columbia University, and* Nagaraj, Krishnaswamy, *Texas Instruments, New Jersey;* and Suyama, Ken, *Columbia University*

In this paper, two possible switched capacitor implementations of companding are discussed. The governing difference equations, an estimate of the increase in the dynamic range for a given power consumption and possible topologies are given.

WAA9-5 -- A New Look at Analogue Computing Using Switched Capacitor Circuits

Sobhy, Mohamed Ibrahim, *The University of Kent at Canterbury, and* Makkey, Mostafa, *The University of Assiut*

The main objective of this work is to develop an analogue computer based on switched capacitor circuits. The system is suitable for solving nonlinear differential equations in real time. This has considerable advantages in solving systems of equations that cannot be solved analytically and of optimising nonlinear systems. The method has been used to solve nonlinear systems for the generation of Solitons and the results have been compared to measurements.

WAA9-6 -- Clocking Scheme for Switched-Capacitor Circuits

Steensgaard-Madsen, Jesper, *Technical University of Denmark*

A novel clocking scheme for switched-capacitor (SC) circuits is presented. It can enhance the understanding of SC circuits and the errors caused by MOSFET (MOS) switches. Charge errors, and techniques to make SC circuits less sensitive to them, are discussed.

WAA9-7 -- Settling Time Design Considerations for SC Integrators

Chilakapati, Uma, and Fiez, Terri, *Washington State University*

Using the general feedback theory, a model is developed to optimize the switched-capacitor (SC) integrator settling time. This model is used to determine the phase margin of the open-loop amplifier to achieve minimum settling time as a closed-loop SC integrator. The sampling switch resistance affects the integrator settling time while the feedback switch resistance has negligible effect.

WAA9-8 -- Recursive Switched-Capacitor Hilbert Transformer

Petraglia, Antonio, *Federal University of Rio de Janeiro*

Efficient implementation of discrete-time Hilbert transformers using switched-capacitor techniques is presented. The proposed network is composed of structurally allpass filters as basic building blocks. As a result, the phase difference of 90 degrees is obtained, for the Hilbert transform pair, with very small sensitivity with respect to capacitance ratio errors. A design example is considered, which includes experimental results obtained in the laboratory with a prototype Hilbert transformer.

WAA10 – Communicating with Chaos III Special Session

Chair: Michael Peter Kennedy

University College Dublin

Organizers: Michael Peter Kennedy

University College Dublin

Geza Kolumban

Technical University of Budapest

Sponsor: Technical Committee on Nonlinear Circuits and Systems

9:00am – 12:30pm - Room: San Carlos I

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA10-1 -- Multiplex Communication Scheme Based on Synchronization via Multiplex Pulse-Trains

Torikai, Hiroyuki, *HOSEI University*; Saito, Toshimicho and Schwarz, Wolfgang, *Dresden University of Technology*

We consider synchronization of more than one pair of chaos systems connected by a single line. First, a master-slave system is introduced and a variety of synchronization phenomena (e.g., synchronization of multiple chaos and of multiple periodic orbits) are discussed theoretically and experimentally. Based on these phenomena, a multiplex communication scheme is discussed.

WAA10-2 -- Synchronizing Autonomous Chaotic Circuits Using Bandpass Filtered Signals

Carroll, Thomas L. and Johnson, Gregg A., *US Naval Research Lab*

The same broad-band properties that make chaos interesting as a potential communications carrier also cause trouble when chaotic signals are transmitted through real communications channels. Phase and amplitude distortion of a chaotic signal can ruin the ability of a chaotic receiver to synchronize to an incoming chaotic signal. We show that it is possible to use narrow band filters with the chaotic signal to reduce its bandwidth, decreasing the effects of channel distortion, and still synchronize a chaotic receiver to the incoming chaotic signal.

WAA10-3 -- Master Stability Functions for Synchronized Chaos in Arrays of Oscillators

Pecora, Louis M. and Carroll, Thomas L., *Naval Research Laboratory*

We show that many coupled oscillator array configurations considered in the literature can be put into a simple form so that determining the stability of the synchronous state can be done by a master stability function which solves, once and for all, the problem of synchronous stability for any linear coupling of that oscillator.

WAA10-4 -- Exploiting the Concept of Conditional Transversal Lyapunov Exponents for Study of Synchronization of Chaotic Circuits

Galias, Zbigniew, *University of Mining and Metallurgy*

The problem of synchronization of coupled chaotic systems is considered. Synchronization is studied by means of local transversal Lyapunov exponents. We show that they can be successfully used in investigations of the synchronization properties. The technique is illustrated with computer simulations.

WAA10-5 -- Nonlinear Hinfinity Synchronization: Case Study for a Hyperchaotic System

Suykens, Johan A.K. and Vandewalle, J., *K.U. Leuven*; Chua, L.O. *University of California at Berkeley*

In this paper we apply the method of nonlinear Hinfinity synchronization to a hyperchaotic system, which consists of two unidirectionally coupled Chua's circuits. This method makes use of a vector field modulation at the master system by a filtered binary valued message signal. Static output feedback is applied to the slave system. The original message is recovered from a tracking error, which is defined after representing the

synchronization scheme in standard plant form according to modern control theory. The controller is designed based upon a matrix inequality, in order to minimize the L2-gain from the exogenous input (message signal and channel noise) to the regulated output (tracking error).

WAA10-6 -- Estimation via Synchronization: FM Demodulation Example

Hahs, Daniel W. and Corron, Ned J., *Dynetics, Inc.*

In this paper, system synchronization is suggested as an approach for state reconstruction and system identification. The potential of this approach is demonstrated by the development and implementation of a simple frequency estimation and tracking system incorporating synchronization. The electronic circuit realization is successfully used to estimate signal frequencies and to track FM waveforms.

WAA10-7 -- Chaos Synchronization in Coupled Phase System

Shalfeev, Vladimir Dmitrievich, *University of Nizhny Novgorod*; Matsrov, V.V. and Korzinova, M.V., *University of California, San Diego*

We demonstrate by computer simulation that the cascade coupled PLLs may be a useful tool for solution of problem of generation and synchronization of chaotic oscillations.

WAA11 – VLSI Layout and Timing

Chair: Majid Sarrafzadeh

Northwestern University

9:00am – 12:30pm - ***Room: San Carlos II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA11-1 -- On Orientation Metric and Euclidean Steiner Tree Constructions

Li, Y. Y.; Leung, K.S.; and Wong, C. K., *The Chinese University of Hong Kong*

We consider Steiner minimal trees (SMT) in the plane, where only orientations with angle $\frac{i\pi}{\sigma}$, $0 \leq i\leq \sigma-1$ and σ an integer, are allowed. The orientations define a metric, called the orientation metric, λ_{σ}, in a natural way. In particular, λ_{2} metric is the rectilinear metric and the Euclidean metric can be regarded as λ_{∞} metric. In this paper, we provide a method to find an optimal λ_{σ} SMT for 3 or 4 points by analyzing the topology of λ_{σ} SMT's in great details. Utilizing these results and based on the idea of loop detection first proposed in [8], we further develop an $O(n^2)$ time heuristic for the general λ_{σ} SMT problem, including the Euclidean metric. Experiments performed on publicly available benchmark data for 12 different metrics, plus the Euclidean metric, demonstrate the efficiency of our algorithms and the quality of our results.

WAA11-2 -- Computational Complexity Analysis of Set-Bin-Packing Problem

Izumi, Tomonorim; Yokomaru, Toshihiko; Takahashi, Atsushi, and Kajitani, Yoji, *Tokyo Institute of Technology*

Given a set of items and a set of bins of the same capacity, the Set-Bin-Packing Problem (SBP) is to pack all the items into the bins where each item is associated with a set and a bin can contain items as long as the number of distinct elements in the union of the sets does not exceed the capacity. One of applications is in FPGA technology mapping, which is our initial motivation .In FPGA terminology, an item, an element in an item, a bin, capacity correspond to a gate, an input signal of a gate, an LUT, and the number of input terminals of an LUT. In this paper, the computational complexity of SBP is studied with respect to three parameters; the number of input terminals of an LUT, the upper bound of the number of input signals of a gate, and the upper bound of the number of fanout gates of a signal, respectively. Our result reveals that SBP remains NP-hard for small values of these parameters. The results are summarized on a 3D map of computational complexities with respect to these three parameters.

WAA11-3 -- A New Approach to Over-the-Cell Channel Routing

Wang, Ting-Chi, *Chung Yuan Christian University*; Wen, Shui-An, *Industrial Technology Research Institute*; Wong, D. F., *University of Texas at Austin*; and Wong, C. K., *Chinese University of Hong Kong*

In this paper, we study the over-the-cell channel routing problem for the cell model in which all the pins are positioned along a horizontal line inside the corresponding cell. We present an efficient approach to the problem under the assumption that two metal layers are available for routing in each of the two over-the-cell regions and three metal layers are available for routing in the channel. The idea of our approach is to treat the three routing regions as a two-layer expanded channel, and to generate a two-layer channel routing solution first. The solution is then transformed into the final over-the-cell channel routing solution with the objective of minimizing the resulting width of the original channel. The transformation problem is reduced to the constrained two-processor scheduling problem for which we develop a polynomial time optimal algorithm. Our approach has been implemented in C language, and experimental results are also provided to support it.

WAA11-4 -- A Heuristic Algorithm to Solve Constrained Via Minimization for Three-Layer Routing Problems

Takahashi, Kazahiro and Watanabe, Toshimasa, *Hiroshima University*

The constrained via minimization problem is the problem of minimizing the number of vias by changing the layer assignment of nets whose routing are given. It has already been known that the problem is NP-complete even for three layer routing. The subject of the paper is to propose a heuristic algorithm VMBF, based on the breadth-first search, to solve the constrained via minimization for the three layer routing problem. Experimental results are provided to show capability of the proposed algorithm.

WAA11-5 -- Utility Function Based Hybrid Algorithm for Channel Routing

Etawil, Hussein A. and Vannelli, Anthony, *University of Waterloo*

This paper presents a two layer channel router with no doglegs, based on a hybridization of Stochastic Evolution and Tabu search methods. The problem-domain knowledge expressed in the form of utility functions is used to guide the exploration of the search space. Unlike previous search heuristic based routers, the use of utility functions in our router provides a powerful tool to determine the best moves that guarantee convergence in shorter times. The algorithm begins with an initial placement of nets, generated such that the nets are relatively in conform with the vertical constraint graph. Vertical and horizontal constraints are observed during the search process. The feasibility of the ideas is demonstrated using five benchmark problems. Optimal solutions are found in each case.

WAA11-6 -- An Age-Controlled Evolutionary Algorithm for Optimization Problems in Physical Layout

Huber, Andreas and Mlynski, Dieter A., *Universitat Karlsruhe*

We present the first evolutionary approach using an age-controlled population model for solving layout problems. In this approach the age is counted individually. Age-intrinsic information and possible conclusions are discussed elaborately. The age-intrinsic information is exploited to improve and accelerate the optimization. Selection and mutation benefit from this approach. Due to industrial needs the optimization characteristic is controlled by a single strategy variable "sigma". This strategy is best-suited for discrete and combinatorial optimization problems. It facilitates efficient controlling of genetic operators. The presented strategy has been implemented and successfully applied to the assignment problem on Analog Transistor Arrays. This paper focuses on the general problem-independent aspects.

WAA11-7 -- Timing Optimization of Mixed Static and Domino Logic

Zhao, Min and Sapatnekar, Sachin, *Univerity of Minnesota*

A timing optimization algorithm dealing with circuits containing mixed domino and static logic is described. Transistor-level node timing constraints of domino logic is described. The optimization procedure preserves the requirements of maintaining adequate noise margins by constraining the sizing procedure. After sizing, charge-sharing problems are identified with a new method and rectified.

WAA11-8 -- Optimizing Circuits with Confidence Probability using Probabilistic Retiming

Tongsima, Sissades; Chantrapornchai, Chantana; and Sha, Edwin H.-M., *University of Notre Dame*; Passos, Nelson L., *Midwestern State University*

VLSI circuit manufacturing results in theoretically identical components that actually have varying propagation delays. A ``worst-case" or even ``average-case" estimation of such delays during the design procedure may be overly pessimistic and will lead to costly and unnecessary redesign cycles. This paper presents a new optimization methodology, called probabilistic retiming, which transforms a circuit based on statistical timing data gathered either from component production histories or from a simulation of the fabrication process. Such circuits are modeled as graphs where each vertex represents a combinational element that has a probabilistic timing characteristic. A polynomial-time algorithm, applicable to such a graph, is developed which retimes a circuit in order to produce a design operating in a specified cycle time within a given confidence level. Experiments show that probabilistic retiming consistently produces faster circuits for a given confidence level, as compared with the traditional retiming algorithm.

WAA12 – Systems and Appls. For Next Generation Internet Special Session

Chair: Chung-Sheng Li

IBM T. J. Watson Research Center

Organizers: Tsu-han Chen

CMU

Chung-Sheng Li

IBM T. J. Watson Research Center

Horng-Dar Lin

NeoParadigm Inc.

Sponsor: IEEE CAS Multimedia Systems and Applications Technical Committee

9:00am – 12:30pm - Room: San Carlos III

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA12-1 -- System Resource Management for Network Servers

Kandlur, Dilip D. *I.B.M. Thomas J. Watson Research Center*

The Internet Engineering Task Force (IETF) is currently in the process of overhauling the architecture of the Internet to meet new challenges and support new applications. One of the most important components of that venture is the enhancement of the Internet service model from a class-less best-effort service architecture to an integrated services architecture supporting a multitude of classes and types of services. In this paper we present an overview of the different services being defined and their intended target applications. We also explore some of the challenges in designing network servers for this environment and present an architecture for system resource management that enables applications to exploit the new services offered by the emerging Internet.

WAA12-2 – Wireless Systems and Portable Multimedia

Lin, Horng-Dar, *NeoParadigm Labs, Inc.*

Next generation networks no doubt will include various types of multimedia data, ranging from real-time news updates to audiovisual multicast events. Multimedia terminals play an integral role in the overall information access fabric. While traditional desktop and settop terminals most likely will continue with the existing technology, portable and wireless multimedia terminals have lots of research and development issues to be solved. This paper starts with reviewing current technology through some existing consumer-grade portable multimedia devices and then investigates various research topics of next generation portable and wireless multimedia access.

WAA12-3 -- Very High-Speed Digital Subscriber Lines (VDSL)

Cioffi, John M., *Information Systems Laboratory*

Very high-speed Digital Subscriber Lines (VDSL) is overviewed with an emphasis on the basic architecture, applications, and data rates, as well as the technological challenges of the design. Discussions of the telephone line environment, radio-band interference ingress and egress, impulse noise, and symmetric and asymmetric multiplexing are included along with the consequent description of a popular implementation.

WAA12-4 -- Issues for Image/Video Digital Libraries

Manjunath, Bangalore S. and Deng, Yining, *University of California at Santa Barbara*

Creation of digital image and video libraries poses several interesting and challenging problems. New tools are needed for managing such multimedia content. These include methods to search, retrieve, and manipulate digital media by using the media content information and mechanisms to protect intellectual property rights. This paper outlines some of the recent advances in image processing as related to digital libraries in the context of the UCSB Alexandria Digital Library project.

WAA12-5 -- Transcoding Internet Content for Heterogeneous Client Devices

Smith, John R.; Mohan, Rakesh; and Li, Chung-Sheng, *IBM T. J. Watson Research Center*

There is a growing diversity of client devices that have access to the Internet. However, much of the content on the Internet cannot be handled by the devices that have limited communication, processing, storage and display capabilities. In order to improve the utility of a wide range of client devices, we propose a network-based solution for transcoding Internet content. The system uses an InfoPyramid for representing and transcoding video, images, audio and text. The InfoPyramid manipulates the content along the dimensions of fidelity and modality, and aggregates the methods for content analysis, translation, filtering and selection. The InfoPyramid utilizes a policy engine, which incorporates user and publisher preferences, various transcoding policies, device descriptions, and real-time network constraints in order to adapt the Internet content to the client devices.

WAA12-6 -- Real-Time Distributed and Parallel Processing for MPEG-4

He, Yong; Ahmad, Ishfaq; and Liou, Ming L., *The Hong Kong University of Science and Technology*

MPEG-4 is currently being developed by MPG to specify the technologies for supporting current and emerging multimedia applications. Because of its object0based features and flexible toolbox approach, it is much more complex than previous video coding standards. We believe that software-based implementation on parallel and distributed computing systems is a natural and viable option. In this paper, we describe such an approach on the MPEG-4 video encoder using a cluster of workstations. We propose to use hierarchical Petri Nets as a modeling tool to describe the temporal relations and time constrains among various video objects at different levels. This would allow us to perform scheduling with a guarantee of synchronization among multiple objects. A dynamic shape-adaptive data parallel approach is used in the spatial domain for further speed-up grain. Our preliminary results indicate that real-time MPEG-4 encoding using distributed and parallel computing is achievable.

WAA12-7 -- Video Coding and Multimedia Communications Standards for Internet

Chen, Tsuhan, *Carnegie Mellon University*

In this paper, we report recent development in video coding and multimedia communications for Internet applications. In the coding aspect, emphasis is given to a number of emerging standards, including H.263 Version 2, H.26L, MPEG-4, and MPEG-7. In the communication aspect, H.323, an ITU-T standard developed for multimedia communications over non-QoS networks, is discussed.

WAA12-8 -- A Virtual Classroom for Real-Time Interactive Distance Learning

Hwang, Jenq-Neng; Deshpande, Sachin G.; and Sun, Ming-Ting, *University of Washington*

With the progress in the digital media (video, audio) compression and multimedia networking, distance learning and media-on-demand applications are rapidly becoming more feasible and accessible. Majority of the distance learning systems can be classified as real-time(live) and non-real-time (stored, on-demand). Each of these categories leads to a different set of constraints and possible solutions. For real time applications the focus is on achieving fast and efficient compression and network delivery of the live contents to the client machines. For on-demand systems, the focus is on embedding various multimedia features and streaming the stored contents to the end user. In this paper, a real-time system under development at the University of Washington is presented.

WAA12-9 -- Fast Browsing of Speech/Audio Material for Digital Library and Distance Learning

Wong, Peter H.W. and Au, Oscar C., *Hong Kong University of Science and Technology*

In digital library and distance learning applications, one usually needs to search through lots of speech materials. While content-based retrieval techniques can help to identify possible matching items, the person would usually need to browse through the items quickly before making decisions on whether the items are useful or not. As a result, fast speech browsing techniques are highly desirable In this paper, we discuss problems of fast playback of speech materials and overview some existing time scale modfification (TSM) techniques. We propose some novel modifications of TSM to make it much more effective in fast browsing of speech materials, especially those with irregular speech tempo. The proposed algorithm includes silent period removal, gain equalization and locally adaptive TSM. Simulation results show that the proposed algorithm can increase the intelligibility of the fast playbacked speech materials significantly.

WAA13 – Digital Filter Design and Implementation

Chair: Y.C. Lim

National University of Singapore

9:00am – 12:30pm - ***Room: Serra Ballroom – Back I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA13-1 -- Efficient Parallel FIR Filter Implementations Using Frequency Spectrum Characteristics

Parhi, Keshab K., *University of Minnesota*

Parallel (or block) FIR digital filters can be used either for high-speed or low-power (with reduced supply voltage) applications. Traditional parallel filter implementations cause linear increase in the hardware cost with respect to the block size. Recently, an efficient parallel FIR filter implementation technique requiring a less-than linear increase in the hardware cost was proposed. This paper makes two contributions. First the filter spectrum characteristics are exploited to select the best fast filter structures. Second, a novel block filter quantization algorithm is introduced. Using filter benchmarks, it is shown that the use of the appropriate fast FIR filter structures and the proposed quantization scheme can result in reduction in the number of binary adders ranging from 4% to 24% and an average reduction of about 10%. Furthermore, the power consumption of these filters is reduced by 14.8% on average and ranges from 10% to 20%.

WAA13-2 -- Signed Power-of-Two (SPT) Term Allocation Scheme for the Design of Digital Filters

Lim, Yong-Chang,and Yang, Rui, *National University of Singapore*;Li, Dongning, *System Technology*; and Song, Jianjian, *National Supercomputing Research Centre*

It is well known that if each coefficient value of a digital filter is a sum of SPT terms, the filter can be implemented without using multipliers. In the past decade, several methods had been developed for the design of filters whose coefficient values are sums of SPT terms. Most of these methods are for the design of filters where all the coefficient values have the same number of SPT terms. In this paper, we present a new method for allocating different number of SPT terms to each coefficient value keeping the total number of SPT terms fixed. Our technique yields excellent results.

WAA13-3 -- Peak-Constrained Design of Non-recursive Digital Filters with High Passband/Stopband Energy Ratio

Netto, Sergio Lima, and Diniz, Paulo Sergio Ramirez, *COPPE - Universidade Federal do Rio de Janeiro*

A new approach for designing nonrecursive digital filters is proposed. The method is able to compromise the minimax efficiency of maximizing the stopband attenuation and the ability of the weighted least-squares (WLS) method to minimize the total stopband energy. The approach uses a time-varying weight function which is made constant, at each iteration, inside a given frequency interval. For that matter, a partially WLS-like and partially equiripple stopband is achieved along with an equiripple passband. Efficient implementations of the new method present computational complexity comparable to minimax-based approaches. Examples are included demonstrating the good results achieved with the proposed scheme.

WAA13-4 -- An Iterative Reweighted Least Squares Algorithm for Constrained Design of Nonlinear Phase FIR Filters

Lang, Mathias C., *Vienna University of Technology*

This paper proposes an iterative reweighted least squares algorithm for constrained designs of FIR filters with arbitrary magnitude and phase responses. The filters are optimum according to a complex constrained least squares or a complex constrained Chebyshev criterion. It is possible to mix the design criteria and different criteria can be used in different frequency bands. The algorithm is computationally efficient and numerically robust. The memory requirement is low because no matrices have to be stored.

WAA13-5 -- Design of Linear Phase FIR Filters Using the Nonuniform DCT

Okuda, Maahiro; Kageyuki, Kiyose; Okuda, Masahiro; Kiyose, Kageyuki; Ikehara, Masaaki; and Takahashi, Shin-ichi, *Keio University*

We propose a novel interpolation technique for the design of linear phase FIR filters on nonuniform frequency grids.

WAA13-6 -- Optimal Fixed-Point VLSI Structure of a Floating-Point Based Digital Filter Design

Wu, An-Yeu and Hwang, Kuo-Fuo, *National Central University*

In this paper, we develop a knowledge-based CAD tool to assist the system IC designers with the fixed-point implementation of a prescribed digital filter. The tool will analyze the finite-precision behavior of three possible fixed-point implementations of a given floating-point based filter design. Based on the analytical results, the tool can suggest most suitable filter structure, wordlength assignment, and scaling operations to realize the filer. It will also estimate the hardware cost of the resulting VLSI architectures. Therefore, the designer can simply pick up the most cost-efficient BLSI implementation of the target filter without going through tedious fixed-point analysis.

WAA13-7 -- Improved Tuning Accuracy Design of Parallel-Allpass-Structures-Based Variable Digital Filters

Stoyanov, Georgi Kostov, *Tohoku University*

The best and simplest method to realize variable IIR digital filters is to apply frequency transformations on a parallel-allpass-structures-based circuit, followed by truncated Taylor series expansions of the allpass sections coefficients. In this work an approach to minimize the two main disadvantages of

this method is proposed. It is shown first, after analyzing the sensitivity of the realization, that the degradation of the stop-band characteristics could be considerably decreased by minimizing the sensitivities of the allpass sections in the parallel structure over some critical frequency ranges. Then the tuning accuracy is improved by minimizing the sensitivities of the allpass sections used to apply the frequency transformations. Appropriate first- and second-order allpass sections are proposed for the most typical cases. The effectiveness of the proposed approach is demonstrated by simulation examples.

WAA13-8 -- Computationally Fast Lattice Bilinear Digital Ladder Filters with Comparison to Circulator WDF's

Harnefors, Lennart, *Malardalen University*

This paper considers a modified variant of the lossless digital integrator lattice filter structure presented in [1,2,3], which in [1] is also labeled lattice bilinear digital ladder filter (BDLF). It is shown that the structure easily can be modified so that the critical loop reduces from two multipliers to one. This has the potential of significantly improving the computational speed when the filter is implemented directly in hardware. Two test filters of the modified BDLF structure are compared to three-port circulator lattice wave digital filters (WDF), which also have critical loops of only one multiplier. It is shown that for the test filters, the BDLF realizations are similar to the WDF realizations regarding multiplier wordlength requirements, while they are superior regarding quantization noise and structural complexity.

WAA13-9 -- Design of General-Order Bode-Type Variable-Amplitude Digital Equalizers

Nowrouzian, Behrooz, *University of Alberta*

The conventional design of Bode-type variable-amplitude digital equalizers is based on the realization of an overall magnitude-frequency response which can be varied from that of a shaping transfer function to its inverse by varying a single variable multiplier over a specified range of values, where the latter range of multiplier values is strongly dependent on the choice of the shaping transfer function. This paper presents a novel approach to the design of arbitrary-order Bode-type variable-amplitude digital equalizers which eliminates the dependence between the range of variable multiplier values and the shaping transfer function. The salient feature of this approach is that it leads to a substantial simplification in the realizability conditions associated with the digital equalizer, and, in turn, leads to a reduction in the cost of the corresponding hardware implementation of the digital equalizer. Moreover, it narrows the variable multiplier values to an effective range which is devoid of impractically large extreme values. The proposed technique is illustrated through its application to the design of a new fourth-order Bode-type variable-amplitude digital equalizer.

WAA13-10 -- A Novel Modified Branch-and-Bound Technique for Discrete Optimization over Canonical Signed-Digit Number Space

Nowrouzian, Behrooz, *University of Alberta*

A novel algorithm is presented for the design of DSP systems by optimization using the branch-and-bound technique over the canonical signed-digit(CSD) multiplier coefficient space. The proposed algorithm has two main salient features:1) For a given infinite-precision decimal floating radix-point multiplier coefficient x, it can directly provide the corresponding decimal floating radix-point values for the smallest representable CSD coefficient greater than x and the largest representable CSD coefficient less than x, where these CSD coefficients have pre-specified wordlength and number of nonzero digits. 2) It does not make any recourse to conversion from CSD to decimal, and vice versa, from decimal to CSD conversion. The proposed algorithm finds applications in the optimization of multi-rate IIR or FIR digital filters over the CSD coefficient space.

WAA13-11 -- Analytical Guess of Error for Nonlinear FIR Filters to Approximate Linear Phase Response

Yagyu, Mitsuhiko, Nishihara, Akinori, and Fujii, Nobuo, *Tokyo Institute of Technology*

This paper presents a method to analytically guess output errors for a type of nonlinear FIR filters to approximate linear phase response. The optimal nonlinear FIR filters generate much smaller output errors than conventional linear FIR filters under the condition of the specified amount of multiplications and additions and are obtained by using an iterative optimization. Using the analytical guess, we can not only estimate the error of the optimal nonlinear filter but also speed up the optimization. We confirm that the analytical guess is accurate in many design examples and the effectiveness of the nonlinear filters in various design specifications.

WAA13-12 -- A Systematic Technique for Designing Approximately Linear Phase Recursive Digital Filters

Saramaki, Tapio Antero, *Tampere University of Technology*

A systematic design method is introduced for synthesizing approximately linear phase lowpass recursive digital filters. Given the amplitude specifications, the filter parameters as well as the slope of the linear phase response are optimized in such a way that the maximum phase deviation from this linear phase is minimized in the passband. The filter structures under consideration are the conventional cascade-form realization of the second- and first-order blocks and the parallel connection of two allpass filters (wave digital lattice filters). There are two different criteria for the transition band behavior of the filter. In the first case, it is required that in the transition band the maximum amplitude value be less than or equal to the passband maximum. In the second case, the amplitude response is required to be monotonously decreasing in the transition band. The overall synthesis technique consists of two basic steps The first step involves finding in a simpler manner a good suboptimum filter. This filter is then used in

the second step as an initial filter for further optimization. The optimization in the second step is performed by properly modifying the Dutta-Vidyasagar algorithms. Several examples are included illustrating the efficiency of the proposed design scheme. They also show the superiority of the resulting recursive filters over their linear-phase FIR equivalents especially in narrowband cases.

WAA13-13 -- Design of Very Low-Sensitivity and Low-Noise Recursive Digital Filters Using a Cascade of Low-Order Wave Lattice Filters

Saramaki, Tapio Antero, *Tampere University of Technology*

One of the best structures for implementing recursive digital filters are the wave lattice filters (parallel connections of two allpass filters). They are characterized by many attractive properties, such as a reasonably low coefficient sensitivity, a low roundoff noise level, and the absence of parasitic oscillations. The main drawback is that if the stopband attenuation is very high, then many bits are required for the coefficient representation. In order to get around this problem, a structure consisting of a cascade of wave lattice filters is introduced in this paper. The main advantage of the proposed structure compared to the direct wave lattice filter is that the poles for the new structure are further away from the unit circle. This means that the number of bits required for the data and coefficient representations are significantly reduced compared to the direct wave lattice filters. The price paid for these reductions is a slight increase in the overall filter order. By properly selecting the number of wave lattice filters and optimizing them, their coefficients can be implemented by a few powers-of-two. Filters of this kind are very attractive in VLSI implementations where a general multiplier is very costly.

WAA13-14 -- Analytical Design of Almost Equiripple FIR Half-Band Filters

Zahradnik, Pavel, Vlcek, Miroslav. *Czech Technical University;* and Unbehauen, Rolf, *University Erlangen-Nurnberg*

A novel analytical design procedure of almost equiripple FIR half-band filters is developed. The design is based on the generating function related to the Jacobi's polynomials. The differential equation for the generating function is presented. A formula for the impulse response coefficients of the filter is derived. One example of the design is included.

WAA13-15 -- Design and VLSI Implementation of Multirate Filter Banks Based on Approximately Linear Phase Allpass Sections

Summerfield, Stephen, *Warwick University*

The design of multirate filterbanks for applications such as subband coding with IIR QMF (quadrature mirror filter) pairs is explored. These offer reduced complexity and low latency at the expense of the loss of exact linear phase. In particular we consider the use of allpass sections where linear phase is approximately achieved by being part of the objective in numerical optimisation. The results for phase distortion in reconstruction experiments compare favourably with previous IIR based approaches. Finite wordlen- gth design using simulated annealing shows that low coefficient wordlengths may be used. This leads to efficient realisations with 3-port adaptors. Using pipelined implementation, a flexible VLSI architecture is designed that can be used for a variety of subband decompositions. Layout and simulation of the design has been performed.

WAA13-16 -- A Highly-Flexible FIR Processor with Scaleable Dynamic Data Ranges

Chen, Oscal T.-C., *National Chung Cheng University*

A highly-flexible finite impulse response (FIR) architecture with scaleable dynamic ranges of input data and filter coefficients is proposed based on the radix-4 Booth algorithm. In order to achieve scaleability, the configurable-connection function between input data latches and filter taps has been explored. The precision of filter coefficients is adjustable by using a path-control function. Especially, the proposed architecture only employs data-path controls to realize the scaleable issue without changing word lengths and components of input latches and filter taps. Based on our architecture, a typical FIR processor with 64-tap 8-bit and 32-tap 16-bit operations was implemented by using the COMPASS 5V cell library in the TSMC 0.6um CMOS technology. Its die size is around 8.0mm * 8.0 mm with a power consumption of 2.9W at a system clock of 100 MHz.

WAA13-17 -- A Computationally Efficient Design of Two-band QMF Banks Based on the Frequency Sampling Approach.

Gandhi, Rajeev, and Mitra, Sanjit, *University of California, Santa Barbara*.

Two new methods for computationally efficient design of two-channel quadrature mirror filter (QMF) banks based on the frequency sampling approach are introduced. In the proposed approach, the number of parameters to be optimized are reduced significantly, thereby leading to a faster design of two-channel QMF banks. The characteristics of the filters obtained are comparable to those of some of the existing QMF banks, in terms of the overall amplitude distortion and the minimum stopband attenuation.

WAA13-18 -- Low Power Implementation of Linear Phase FIR Filters for Single Multiplier CMOS Based DSPs

Erdogan, Ahmet Teyfik *Cardiff University of Wales,*

Recently, a new scheme for the single multiplier implementation of low power digital filters on CMOS-based DSPs was presented [1,2]. In this paper the scheme is generalised to include linear phase FIR filters (LPFIRs) and its implementation is investigated with two common methods of LPFIR realisation structures. The paper also describes an effective framework which combines layout, timing, and capacitive information, for the evaluation of power consumption for FIR filters. New results are provided which demonstrate up to 85% reduction in overall power consumption. The paper

discusses the generalisation of the scheme to LPFIRs and the effects of added overheads, describes the evaluation environment, and provides comprehensive results which show the effectiveness of the scheme as a generic power saving framework for the implementation of FIR filters exploiting coefficient symmetry, where exists, without the need for specialzsed realisation structures.

WAA13-19 -- Automated Design of Low Complexity FIR Filters

Redmill, David Wallace, and Bull, David R., *University of Bristol*

This paper considers the design of low complexity FIR filters. Complexity is reduced by constraining the filters to have integer coefficients, which can be efficiently implemented using primitive operator directed graphs (PODG). Genetic Algorithms (GAs) are used in conjunction with a heuristic graph design algorithm, to provide a solution set which represents different compromises between performance, complexity and filter order. Example results are presented for both one and two dimensional filters, and are shown to provide both superior performance and complexity, compared to previous methods. The main benefits result from the use of a joint optimization, rather than a separable 2-stage approach. The use of a PODG representation is shown to provide significant improvements over a canonic signed digit (CSD) or signed power-of-two (SPT) representation.

WAA13-20 -- Architecture of a Programmable FIR Filter Co-Processor

Gay-Bellile, Olivier, Dujardin, Eric, *Laboratoires d'Electronique Philips S.A.S.*

This paper presents a new generic architecture to build co-processors dedicated for FIR filtering algorithms, which can implement a set of different filter like symmetric and adaptive filters with or without decimation. Moreover, it manages various types of data (real or complex) and different data accuracies (8 or 16 bits) owing to a specific operative bloc architecture. For instance, a 60.000 equivalent gates co-processor is described that copes with a 512-tap symmetric filter in 8-bit accuracy with a working frequency of 100 MHz (the computation power is 4.8 Gops). So, it could be used as a powerful co-processor for new generation DSPs as Philips TriMedia and Texas Instruments TMS320C6201 whenever filtering functions are required as in digital communications.

WAA13-22 -- Digital Hilbert Transformers Composed of Identical Allpass Subfilters

Johansson, Hakan, and Wanhammar, Lars, *Linkoping University*

In this paper we introduce digital Hilbert transformers composed of identical allpass subfilters that are interconnected via extra multipliers. In the simplest case the overall transfer function corresponds to M Hilbert transformers in cascade where each transformer is derived by frequency shift of a half-band IIR filter. The overall transformer can also be designed to have a smaller passband ripple than for a pure cascade design. The values for the extra multipliers are computed using simple recurrence formulas. One advantage of the proposed structures if that the sensitivity of coefficient errors of the recursive parts, i.e. of the allpass subfilters, are lower than for the corresponding conventional structures. One consequence of this is that the maximal sample frequency is higher for the new structures. Since the coefficients of the allpass subfilters in the new structures are shorter, the overall arithmetic complexity can under certain conditions also be reduced. Examples are included that demonstrate this.

WAA13-23 -- Data Block Processing for Low Power Implementation of Direct Form FIR Filters on Single Multiplier CMOS DSPs

Erdogan, Ahmet Teyfik, *Cardiff University of Wales,*

In this paper, the authors propose a block processing scheme for low power implementation of FIR filters on single multiplier CMOS based Digital Signal Processors (DSPs). The authors show that the reduction in overall power is due to a decrease in switching activity at coefficient inputs of the multiplier and both data and coefficient memory buses by a factor determined by the data input block size. Results are presented which demonstrate up to 34% savings in power. The paper presents the scheme, outlines its implementation using an example and demonstrates results with various filter orders and wordlenghts.

WAA13-24 -- Constrained Genetic Algorithm Design of Finite Precision FIR Linear Phase Raised Cosine Filters

Al-Hashimi, B. M., Somerset, W.P. and Moniri, M. *Staffordshire University*

This paper investigates the use of genetic algorithm in the design of finite wordlength linear phase raised cosine FIR filters. The design of such filters does not only involve meeting a specific amplitude response but also imposes time domain constraints on the impulse response in order to ensure zero intersymbol interference (ISI). It is shown that genetic algorithm provides simple and effective technique for the design of finite precision filters with both frequency and time domain constraints. Furthermore, the algorithm computational time is low with respect to filter order and is independent of word length. Two filter design examples are included demonstrating the effectiveness of the design method.

WAA14 – VLSI Architectures, Algorithms and CAD

Chair: Ken Suyama

Columbia University

9:00am – 12:30pm - ***Room: Serra Ballroom – Back II***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA14-1 -- Accuracy Analysis of Layout Parasitic Extraction Based on Boolean Methods

Brambilla, Angelo, *Politecnico di Milano* and Mancini, Paolo, ***Accent Srl***

Layout parasitic extraction methods based on boolean operation of layers are well established in the design practice. They are developed on hypotheses that the layout can be considered as a two dimensional structure and that net capacitances depand only on the net area and perimeter values. In the paper, we show with the aid of layout structures that these hypotheses are not more valid for submicron layout technology and thus relevant errors are introduced in the estimation of the net capacitances.

WAA14-2 -- Hardware Efficient Transform Designs with Cyclic Formulation and Subexpression Sharing

Chang, Tian-Sheuan and Jen, Chein-Wei, *National Chiao-Tung University*

This paper presents a hardware efficient architecture for transform designs. Unlike other designs that use systolic array and memory-based design, the proposed architecture exploited the constant property of the transform coefficients as well as their numerical property. The proposed design reformulates the transform with cyclic convolution such that filter type subexpression sharing can be applied to reduce the area cost. The results show that the new designs can save up to 81% gate area cost compared with previous designs for 5-point DFT designs.

WAA14-3 -- A Field Programmable Gate Array Chip with Hierarchical Interconnection Structure

Lai, Yen-Tai, Kao, Chi-Chou, Chang, Tsun-Chen, and Chen,Kun-Nern, *National Cheng-Kung University*

This paper presents the architecture and implementation of a field programmable gate array chip with hierarchical interconnection structure. The new field programmable gate array has higher performance than conventional field programmable gate arrays. Its advantages are high density, fast speed, and the flexibility to fit designs into the architecture quickly. The schematic circuit of the FPGA is described, and its layout by using full-customer top-down method is presented.

WAA14-4 -- Low-Energy Programmable Finite Field Data Path Architectures

Song, Leilei and Parhi, Keshab K., *University of Minnesota;* Kuroda, Ichiro and Nishitani, Takao, *NEC Corporation*

This paper considers implementation of finite field multiplication data paths in a domain-specific programmable digital signal processor (DS-PDSP), where special hardware units and corresponding instructions are assumed to be used to program finite field multiplication operation. These multiplication data paths are designed to accommodate programmability with respect to the primitive polynomial as well as the field order. Three types of multipliers are considered;these include semi-systolic array (in both least-significant-bit first and most-significant-bit first modes), fully-parallel, and the proposed approach where polynomial multiplication and polynomial modulooperations are implemented separately and two instructions, MAC and DEGRED are assigned to them, respectively. Two approaches are considered for achieving programmability with respect to the field order, either with special control circuitry, or with pre- and post-logical shifting operations. It is concluded that the one-level pipelined fully-parallel multiplier without control circuitry consumes the least energy at component level when only one multiplication is considered. However, at system level, when vector-vector multiplications, common in many DSP algorithms, are considered, the proposed approach is able to achieve 70% energy reduction at the expense of increasing the total instruction count by one.

WAA14-5 -- The LEMMA Developer's Toolbox: Semi-Automated Test Development for Analog and Mixed-Signal Circuits

Kennedy, Michael Peter, *University College Dublin*, Grogan, Paul; O'Donnell, John, and O'Dwyer, Tom, *Analog Devices;* Wrixon, Adrian, *University of California, Berekeley*

Analog test represents an increasing fraction of the cost of producing analog and mixed-signal integrated circuits. While digital testing can focus on identifying spot defects in a systematic manner, analog functional testing requires very precise and accurate measurements. Pessimistic forecasts suggest that "in the next few years the total product cost of a mixed-signal device will be almost entirely due to the cost of the analog tests." The LEMMA method is a model -based approach to minimizing the analog test effort by identifying a robust minimum set of testpoints.

WAA14-6 -- An High Speed VLSI Architecture for Scaled Residue to Binary Conversion

Cardarilli, Gian Carlo; Re, M.; Lojacono, R., *University of Rome "Tor Vergataa"*, Ferri, G., *University of L'Aquila*

The scaled Chinese Remainder Theorem (CRT) is a very useful tool for the simplification of RNS to binary converters. The main drawback of this methodology is related to the use of large look-up tables that store the correspondence among the modular numbers and the corresponding scaled terms of the CRT. This fact limits the maximum speed allowed by this approach. In this paper a new method for the computation of the scaled factors is presented. It allows the computation of the scaled CRT output by using very small look-up tables implemented by conventional logic and simple and fast structures, that work in parallel. The only assumption done in order to develop the new algorithm is that the moduli must be odd.

WAA14-7 -- VLSI Implementation of Phong Shader in 3D Graphics

Shin, Yun Chul; Lee, Jin-Aeon; and Kim, Lee-Sup, *Korea Advanced Institute of Science and Technology*

With continuous improvement of VLSI technologies and request of higher realism, real-time Phong shading will be the next technology-push in 3D graphics. Taylor series approximation is appropriate for hardware implementation of Phong shading. We determined hardware size of Taylor series approximation in terms of hardware minimization through visual comparison and implemented Taylor series approximation in a 3-stage pipelined architecture.

WAA14-8 -- State Encoding for Low Power Embedded Controllers

Daldoss, L., *Universita di Brescia*; Sciuto, Donatella, *Politecnico di Milano;* Silvano, C., *Politecnico di Milano*

Power dissipation has become one of the main issues during embedded systems design, due to the continuous increase of the integration level and the operating frequency. The present paper approaches the problem of reducing power dissipation in embedded controllers represented as Finite State Machines (FSMs). The aim of the work is to propose an approach to optimize state encoding for low power embedded FSMs, starting from a probabilistic description of the FSMs. Experimental results have been obtained by applying the proposed state encoding techniques to benchmark circuits. The results have also been compared to previous state encoding methods.

WAA14-9 -- Design of a Scan Line Image Processor Chip

Chang, Hyunman; Ong, Soahwan; Lee, Changhee; and Sunwoo, Myung H., *Ajou University*

This paper describes a linear array image processor chip called the SliM-II Image Processor. The chip has 64 processing elements (PEs) connected by a linear array. In contrast to existing array processors, each PE has a multiplier that is quite effective for convolution, template matching, etc. The instruction set can execute an ALU, a data I/O, and an inter-PE communication operations simultaneously in an instruction cycle. In addition, during the ALU/multiplier operation, SliM-II provides parallel data load/store between the register file and on-chip memory as in DSP chips. The SliM-II chip has been implemented, which contains about 1.5 million transistors in a 13.2 X 13.0 mm2 die size and the package type is 208 pin PQ2. The performance estimation shows a significant improvement compared with existing array processors.

WAA14-10 -- An Efficient Programmable 2-D Convolver Chip

Chang, Hyun Man and Sunwoo, Myung H., *Ajou University*

This paper proposes a new real-time 2-D convolution filter architecture to reduce the product of the hardware complexity and propagation delay. To meet the real-time image-processing requirement, several commercial 2-D convolver chips have many parallel multipliers, which occupy a large VLSI area. The implemented chip uses only one special shift-and-accumulator block instead of nine parallel multipliers. Hence the chip can reduce the chip size by more than 50% of existing 2-D convolvers. Moreover, due to a finite state machine, which is controlling input data sequences, the proposed chip does not require row buffers to store three row image data used in the commercial chips. We used the SOG cell library (KG60K). The implemented filter chip consists of only 3,893 gates, operates at 125 MHz and can meet the real-time image processing requirement, i.e., the standard of ITU-R BT.601.

WAA14-11 -- Synthesis of Folded Multidimensional DSP Systems

Sundararajan, Vijay and Parhi, Keshab K., *University of Minnesota*

In this paper a novel multi-dimensional (MD) folding transformation technique is formalized which can be used to synthesize control circuits for pipelined architectures which implement a specific class of MD DSP algorithms. Feasibility constraints are derived for folding a 2-D single rate data flow graph (DFG) onto an available set of hardware functional units according to a given schedule. Retiming is introduced as a tool to facilitate feasibility of the folding constraints and minimization of the storage requirements for the folded architecture. Detailed design example of a non-separable 2-D IIR filter is provided.

WAA14-12 -- Low Power Scheduling with Resources Operating at Multiple Voltages

Shiue, Wen-Tsong and Chakrabarti, Chaitali, *Arizona State University*

This paper presents (i)a resource-constrained scheduling scheme and (ii)a latency-constrained scheduling scheme that minimize power consumption for the case when the resources operate at multiple voltages. The resource-constrained scheduling reduces the power consumption by maximally utilizing resources operating at reduced voltages and at the same time reducing the latency. The latency-constrained scheduling scheme reduces the power consumption by assigning as many nodes (of the data flow graph)as possible to the resources operating at reduced voltages. Both schemes use heuristics to reduce the power consumed by the level shifters. Two cases have been studied: one in which the possible operating voltages are 5V and 3.3V, and the other in which the operating voltages are 5V, 3.3V and 2.4V. Experiments with HLS

benchmark examples show that the proposed schemes achieve significant power reduction. Keywords: Low Power design, Behavior Synthesis, Scheduling.

WAA14-13 -- A CPLD Design of a Self-Organizing System for Data Clustering

Ohkubo, Jun'ya; Miyanaga, Yoshikazu; and Tochinai, Koji, *Hokkaido University*

A hardware design of a self-organizing system is presented in this report. A high performance parallel processor is designed with pipeline modules. The size of this system is programmable within a certain degree. In this report, we design this system using a target CPLD. In addition, this report shows the error analysis of floating-point operation to estimate the optimum word length of data for the minimization of circuit resources.

WAA14-14 -- High Performance Cell for Solving Real Time Field Problems Using the Resistive Grid Method.

Carneiro, Noel Carlos F. and Ramírez-Angulo, Jaime, *New Mexico State University*

In this paper, we describe a VLSI analog system that simulates a resistive grid and is suitable for applications in real time such as image processing and differential equations solving. The system uses the basic cell configuration described in this paper. Differently from a CNN (-UM) cell, each cell can be individually configured. Besides, each cell has a photo sensor circuit, which allows it to be used in image processing applications.

WAA14-15 -- VLSI Design of a CORDIC-based Derotator

Ahn, Youngho; Nahm, Seunghyeon, and Sung, Wonyong *Seoul National University*

A derotator VLSI which removes the frequency and phase errors of a received signal in digital receivers was developed using a CORDIC algorithm. The CORDIC circuit directly rotates the input signal according to the phase error information, thus is much simpler than the conventional derotator architecture which consists of a DDFS (Direct Digital Frequency Synthesizer) and a complex multiplier. In order to improve the operating speed without employing the pipelining, a fast direction sequence generation method that exploits the linearity of the tangent function in small angles is utilized. The newly employed direction sequence generation method needs only about a third of the iterative computations when compared with the conventional CORDIC algorithm. The chip was designed and implemented using a 0.6 um triple metal CMOS process by the full custom layout method. The whole chip size is 6.8 mm^2 and the operating frequency which is higher than 25 MHz is achieved.

WAA14-16 -- Theoretical Estimation of Power Consumption in Binary Adders

Freking, Robert A. and Parhi, Keshab K., *University of Minnesota*

This paper presents a novel approach for theoretical estimation of power consumption in digital binary adders. Closed-form expressions for power consumption of four different types of binary adders -- the ripple-carry adder, the Manchester adder, a multiplexor-based carry-select adder and an efficient tree-based look-ahead adder -- are derived in terms of word-length and pre-computed technology-specific energy parameters. These expressions are verified to be accurate to within 1 - 5% by simulation using the HEAT tool.

WAA14-17 -- Implementation of the Fuzzy Art Neural Network for Fast Clustering of Radar Pulses

Cantin, Marc-Andre, *Universite du Quebec a Montreal*; Blaquiere, Yves, *Universite du Quebec a Montreal*; Savaria, Yvon and Granger, Eric, *Ecole Polytechnique de Montreal*; Lavioe, Pierre, *Defense Research Establishment Ottawa*

A real time radar signal clustering problem is resolved by a dedicated hardware implementation of the fuzzy art neural network. this novel architecture implements a reformulated algorithm for high speed clustering. the proposed dedicated digital vlsi system is composed of cascadable integrated circuits, each one containing several neural processors, comparators, a divider and blocks of ram. this efficient solution was designed and will be implemented in the near future. The basic component requires 74K gates and occupies an area of 52.5mm2 in a 0.8um bicmos technology. each chip process an input pattern for 32 neurons every 2us.

WAA14-18 -- Neural Core Module for Embedded Intelligence

Diepenhorst, Marco; Ter Haseborg, Henrickus; Nijhuis, J.A.G; and Spaanenburg, L., *University of Groningen*

A multiplication unit is proposed that allows for an efficient computation of products of 32-, 16- and 8-bit fixed point numbers. In the latter two modes of operation, two resp. four multiplications are executed in parallel. The proposed unit implements multiplication according to the DIGILOG principle and is designed to operate on a 100 Mhz clock in a 0.8 mm2 CMOS technology. The design of the unit is motivated by the potential benefits to be gained from a digital platform that integrates the emulation and training of neural networks with pre-processing of the signals that they process. Efficient realization of the multiplication operation is a major requirement of such a device.

WAA14-19 -- Cheap and Easy Systematic CMOS Transistor Mismatch Characterization

Serrano-Gotarredona, Teresa and Linares-Barranco, Bernabe, *National Microelectronics Center*

This paper presents a `do-it-yourself' methodology for characterizing the random component of transistor mismatch in CMOS technologies. The methodology is based on the design of a special purpose chip which allows automatic characterization of arrays of NMOS and PMOS transistors of different sizes. Up to 30 different transistor sizes were implemented in the same chip, sweeping transistors width W and length L. The standard deviation of the mismatch of these parameters is computed (, ,) for each transistor type and size, as well as the statistical correlation factors between

them. These standard deviations and correlations are fitted to two dimensional surfaces so that their values can be predicted as a function of transistor sizes. These functions are used in an electrical circuit simulator (Hspice) to predict transistor mismatch. Measured and simulated data are in good agreement.

WAA14-20 -- Self--Calibrating Clock Distribution with Scheduled Skews

Hsieh, Hong-Yean, *Next Wave Technology Inc.*, Liu, Wentai; Clements, Mark; and Franzon, Paul, *North Carolina State University*

This paper presents a self--calibrating clock distribution scheme that dynamically compensates manufacturing and environmental variations to minimize unintentional clock skews and employs non-zero intentional skews to improve system performance. The tracking process is implemented with an all--digital phase--locked loop and has been verified through a prototype chip. Test results confirm the theoretical predictions that the absolute value of unintentional skew is limited to Delta, which is the resolution of the sampling and compensation circuitry.

WAA14-21 -- Array Architecture and Design For Image Window Operation Processing ASICs

Li, Dongju; Jiang, Li; Isshiki, Tsuyoshi; and Kunieda, Hiroaki, *Tokyo Institute of Technology*

In this paper, we present a novel architecture named as Window-MSPA architecture which targets to window operations in image processing, as an extension of MSPA architecture. We have previously developed a Memory Sharing Processor Array (MSPA) for fast array processing with regular iterative algorithms [1] [2] [3]. Window-MSPA consists of Window-PEs which performs window operations. It minimizes the data I/O ports and the number of Window-PEs. The image data imput scheme is restricted to row by row imput lines which simplifies the I/O architecture. Under this practical I/O restriction, the fastest processings are achieved. The architecture can be used for not only conventional image filtering, but practical window operation such as motion vector search in MPEG2. The derived architecture is flexible enough to adjust user's requirements for either area or speed.

WAA14-22 -- Novel Digit-Serial Systolic Array Implementation of Euclid's Algorithm for Division in GF(2^m)

Guo, Jyh-Huei and Wang, Chin-Liang, *National Tsing Hsu University*

In this paper, a novel digit-serial systolic array for computing divisions in GF(2m) over the standard basis is presented. To the authors' knowledge, this is the very first digit-serial systolic divider for GF(2m). The proposed architecture possesses the features of regularity, modularity, and unidirectional data flow. Thus, it is well suited to be implemented using VLSI techniques with fault-tolerant design. One important feature of the proposed architecture is that different throughput performances can be easily achieved by varying the digit size. By choosing the digit size appropriately, the proposed digit-serial architecture can meet the throughput requirement of a certain application with minimum hardware.

WAA14-23 -- VLSI Architectures of Divider for Finite Field GF(2^m)

Wei, Shyue-Win, *Chung-Hua University*

A cellular-array power-sum circuit for GF(2m) is presented. According to the basic cellular-arra6y power-sum circuit, several VLSI architectures that can be used to compute inversions and divisions over GF(2m) are proposed. Both computation speed and circuit complexity of the presented new divider can be improved by comparing with existing systolic circuits.

WAA14-24 -- A High Throughput Variable Length Decoder with Modified Memory Based Architecture

Shieh, Bai-Jue; Lee, Yew-San; and Lee, Chen-Yi, *National Chiao Tung University*

Variable-Length Code (VLC) is the most popular data compression technique. Therefore, a high throughput Variable-Length Decoder (VLD) is required in many applications. In this paper, we propose 2 simple modified methods which can increase throughput of memory-based two-bit structure Variable-Length Decoder system [1]*. The additional hardware of modified architehture is some control unit and a little memory space. The overall system still consists of control unit, arithmetic unit and memory. Simulation results show that the decompression rate based on 0.6um CMOS process and MPEG2 coding table-15 can achieve720M bits/s with 100 MHz clock rate.

WAA15 – CAD II

Chair: Ibrahim Hajj

University of Illinois

9:00am – 12:30pm - ***Room: Serra Ballroom – Back III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAA15-1 -- A Matlab Based Tool for Bandpass Continuous-Time Sigma-Delta Modulators Design

Benabes, Philippe; Aldebert, Patrick; and Kielbasa, Richard, *SUPELEC*

A methodology for synthesis and analysis of bandpass sigma-delta converters has been developed and integrated in a Matlab toolbox. It allows to synthesize Sigma Delta modulators with continuous time filters from discrete time topologies. The analysis method is based on discretization of continuous-time models. It uses a discrete time simulator, more efficient than an analog simulator. All tools are included in a fully interactive, graphic and open framework in which user-developed modules can be added up.

WAA15-2 -- BiCMOS versus CMOS Technology in Fully Differential OTA Designs

Recoules, Hector; Bouchakour, R.; and Loumeau, P., *Ecole Nationale Superieure des Telecommunications*

A design program evaluates CMOS and BICMOS fully differential OTA's performances independently of the application. As a validation an amplifier has been realized. Measurements and simulations are shown and compared. Finally a comparison is presented between CMOS and BICMOS OTA when long or short transistor lengths are used.

WAA15-3 -- Analysis of Modulator Circuits Based on Multi-Dimensional Fourier Transformation

Ushida, Akido; Yamagami, Yoshihiro, and Nishio, Yoshifumi, *Tokushima University*

There are many communication circuits driven by multitone signals such as modulator and mixer. If the input frequency components are largely different in each other, the brute force numerical method will take and enormous computation time to get the steady-state response. In this paper, we show a SPICE oriented algorithm based on multi-dimensional Fourier transformation, where all of the circuit analyses such as dc- and ac-analysis in the algorithm are carried out with SPICE. On the other hand, a very simple sensitivity analysis and 2-dimensional FFT are carried out by a Fortran program (or C program). We found that the convergence ratio of our algorithm is sufficiently large, and can be applied to wide class of communication circuits.

WAA15-4 -- Joint Optimization of Multiple Behavioral and Implementation Properties of Analog Filter Designs

Damera-Venkata, Niranjan and Evans, Brian L., *The Univerity of Texas at Austin*; and Lutovac, Miroslav D. and Tosic, Dejan V., *University of Belgrade*

This paper presents an extensible framework for optimizing analog filter designs for multiple behavioral and implementation properties. We demonstrate the framework using the behavioral properties of magnitude response, phase response, and peak overshoot, and the implementation property of quality factors. We represent the analog filter in terms of its poles and zeroes. We match the constrained non-linear optimization problem to a sequential quadratic programming (SQP) problem, and develop symbolic mathematical software to translate the SQP formulation into working MATLAB programs to optimize analog filter designs. The automated approach avoids errors in algebraic calculations and errors in transcribing the mathematical equations in software. The packages are freely distributable.

WAA15-5 -- New Description Language and Graphical User Interface for Module Generation in Analog Layouts

Wolf, Markus; Kleine, Ulrich; and Schulze, Jens, *University of Magdeburg*

This paper presents a new description language and a graphical user interface for a module generator environment. The description language MOGLAN is adapted to the problem of writing analog module generators and provides an easy-to-read, short source code. The graphical user interface supports the writing, translating, executing, and debugging of modules. With these tools, analog designers are able to write module generators and to bring in their analog specific knowledge. This increases the quality of automatic layout solutions and decreases the time consuming process of manual layout generation.

WAA15-6 -- Analysis and Compensation of OTA Non-Ideal Effects in Video-Frequency CMOS sinc (x) Equalizers

Dudek, Frank; Al-Hashimi, Bashir M.; and Moniri, M., Staffordshire University

This paper presents a detailed analysis and minimization of OTA non-ideal effects in the performance of sinc(x) equalizers operating at video-frequencies. To compensate these effects, a set of equalizer design equations, expressed in terms of the active devices input capacitance, output resistance and the polynomial coefficients used to correct the sinc(x) distortion is derived, facilitating the synthesis process. Simulation based on CMOS OTAs demonstrates the effectiveness of the design equations in compensating accurately the error introduced by the OTAs in the ideal equalizer. This is demonstrated with reference to a D/A converter with sampling rate of 27MHz over 10MHz bandwidth.

WAA15-7 -- Adjoint Network of Periodically Switched Linear Circuits

Yuan, Fei and Opal, Ajoy, *University of Waterloo*

This paper presents a general theory of the adjoint network of multiphase periodically switched linear (PSL) circuits in frequency domain. The phasor representation of Tellegen's theorem for PSL circuits in steady-state is introduced and the adjoint networks of elements typically encountered in PSL

circuits are developed. It is shown that the transfer functions from multiple input sources to one of a PSL circuit can be computed efficiently by solving the adjoint network of the circuit only once. More importantly, it is demonstrated that the aliasing transfer functions from the input sources in the side bands to the output in the base band can be obtained efficiently by computing the corresponding high-order frequency components of the response of the adjoint network of the circuit.

WAA15-8 -- Layout Driven Macromodel of an Operational Amplifier

Chung-Yuk, Or, *The Chinese University of Hong Kong*Franca, Jose E., *Instituto Superior Tecnico*

This paper describes the generation of the macromodel of an operational amplifier from the layout database. Unlike traditional schematic based macromodels ,this makes it possible to capture all the complex parasitic effects in the layout and hence providing a more accurate representation of the database submitted to fabrication. Results show that such macromodel provides a much faster simulation than the simulation of the netlist extracted from the layout and yet achieves close accuracy with the latter. Therefore, the proposed layout-driven macromodel allows the practical simulation of large layout databases of mixed-signal systems containing in a more time-efficient and accurate manner than can be presently achieved.

WAA15-9 -- On the Algebraic Reuse of Hardware Design

de Melo, Ana Cristina Vieira, *State University of Sao Paulo (USP)*

The widespread use of computers in a diversity of activities today demands complex computational systems to be produced efficiently. This factor has led to a requirement for new methods and techniques to enhance controllability, quality and productivity of systems. Reusability is a basic principle for enhancing productivity and quality of engineering products. Additionally, formal development of software/hardware ensure quality and help handle the complexity of description of such systems. This paper presents a foundation for formal reuse of synchronous processes using a process algebra. Assuming the existence of a library of formally verified components, we propose to make effective reuse of these existing elements when creating new systems. The strategy used here is to formally create an interface element with which a library process is composed in order to implement the desired component. In doing so, the verification task of the whole system is reduced to reasoning about the interface element.

WAA15-10 -- Assessing the Uniqueness of the DC Solution by Tearing of Cactus Graphs via Detection of Hinging Structures

Sarmiento-Reyes, Arturo and Bernal Rafael Vargas, *INAOE*

Cactus graphs are used to determine wheteher or not a circuit may posses multiple dc solutions. This work introduces a tearing method for cactus graphs that can be used to decompose the initail cactus into smaller cactus subgraphs which are hinging altogether. The method is focussed on circuits containing independent current and voltage sources, positive linear resistors, and BJTs, but it can be easily modified in order to cope with devices that can be modelled by equivalent circuits composed by coupled branches. Besides, the concept of path-matrices is introduced in order to determine if the whole graph of the circuit can be split into subgraphs. In a further step, the subgraphs can be analysed separately in order to detect multiple dc operating points.A

WAA15-11 -- On the High Level Canonical Representation of Piecewise Linear Functions

Julián, Pedro; Desages, Alfredo; and Agamennoni, Osvaldo, *Universidad Nacional del Sur*

In this work we propose a representation basis for the set of PWL functions f: D --> R1 defined over a simplicial partition when D is a rectangular compact set in R2. The functions of the basis exhibit several types of nested absolute value functions. In addition, an efficient numerical method is given for the resolution of the parameters of the High Level Canonical representation.

WAA15-12 -- Hierarchical Symbolic Analysis of Large Analog Circuits with Determinant Decision Diagrams

Tan, Xiangdong and Shi, C.-J. Richard, *University of Iowa*

A new hierarchical approach is proposed to symbolic analysis of large analog circuits. The key idea is to use a graph-based representation, called Determinant Decision Diagram (DDD), to represent the symbolic determinant and cofactors of the MNA matrix for each subcircuit block. By exploiting the inherent sharing and spasity of symbolic expressions, DDD is capable of representing a huge number of symbolic product terms in a canonical and highly-compact manner. Further, it enables cofactoring and sensitivity computation to be performed with time linear in the size of DDD. Experimental results have demonstrated that our method outperforms the best-known hierarchical symbolic analyzer SCAPP and even numerical simulator SPICE for small-signal AC analysis.

WAA15-13 -- Reducing Operation Complexity in Symbolic Techniques through Partitioning

Cabodi, Gianpiero; Camurari, Paolo; and Quer, Stefano, *Politecnico di Torino*

Binary Decision Diagrams (BDDs) are the state-of-the-art core technique for the symbolic representation and manipulation of Boolean functions, relations and finite sets. Many applications resort to them in the field of CAD, but size and time complexity are a strong limitation to a wider applicability .In this paper we primarily address the problem of memory limits. In particular, we first include an experimental observation

of memory usage and running time for some basic operators used in reachability analysis of Finite State Machines. Then we describe how disjunctive partitioning allows us to decompose large problems into sub-problems. Finally, we show the benefits in terms of memory requirements, CPU time, and overall performance.

WAA15-14 -- Waveform Approximation Technique in The Switch-Level Timing Simulator BTS

***Chang, Mao-Lin (Molin); Chen, Wang-Jin*, National Taiwan University*; Wand, Jyh-Herng*, National Center for High-Performance Computer*; Feng, Wu-Shiung*, National Taiwan University**

In this paper an accurate and efficient switch-level timing simulator is described. The high accuracy is attributed to a new waveform approximation technique, which includes delay estimation and slope estimation. Efficient delay and slope calculations are accomplished through a switch-level simulation instead of using a transistor-level simulation. A new approach for delay estimation is presented, and it models the delay behavior of an RC tree by two equations: a dominant delay equation and an offset delay equation. Both are derived by a special process to fit the surface built by experimental data measured from the actual delay behavior of a CMOS gate. The results show good agreement with SPICE.

WAA15-15 -- New and Efficient Method for the Multitone Steady-State Circuit Simulation

Larcheveque, Remi and Bolcato, P., *ANACAD EES / MGC*; Ngoya, E., *IRCOM*

A new method termed Compressed Time is presented to compute the steady-state response of nonlinear circuits with periodic or quasi-periodic excitation. It is different from standard or enhanced Shooting method or Harmonic Balance (HB) and allows the simulation of large systems such as large circuits and large number of harmonics. It is based on a time domain formulation of HB equations written in a preconditioned form. The generated system is then solved with a nonlinear block relaxation algorithm. Performances and simulation results are shown for a typical RF circuit.

WAA15-16 -- Generalized Centers of Gravity Algorithm for Yield Optimization of Integrated Circuits

Keramat, Mansour and Kielbasa, Richard, *SUPELEC*

The aim of Design Centering is to minimize or even eliminate the undesirable effect of manufacturing process variations by changing the designable parameter values. The Centers of Gravity (CoG) algorithm is a yield optimization algorithm that was originally developed on a heuristic basis for discrete component circuits. In this contribution, the generalized CoG algorithm which can be applied to integrated circuits is presented.

WAA15-17 -- Statistical Design of Integrated Circuits Using Maximum Likelihood Estimation of the Covariance Matrix

Seifi, Abbas; Vlach, J.; and Ponnambalam, K., *University of Waterloo*

A new formulation is proposed for statistical design of integrated circuits with correlated input parameters. The method uses a polyhedral approximation of the feasible region and finds the maximum volume ellipsoid contained in that polyhedron. The orientation of the ellipsoid is fixed by a maximum likelihood estimate (MLE) of the correlation matrix. The ellipsoid center is a nominal design with the maximum yield. The covariance estimation is formulated as a semidefinite program which uses the sampling observations as input data. The design centering problem is presented as a second-order cone programming and solved by a special interior-point optimization algorithm. The optimal design of a switched-capacitor filter is presented.

WAA15-18 -- Modeling the Dynamic Behavior of Series-Connected MOSFETs for Delay Analysis of Multiple-Input CMOS Gates

Bisdounis, Labros and Koufopavlou, Odysseas, *University of Patras*

In this paper the dynamic behavior of series-connected MOSFETs is studied, in order to compute the propagation delay of multiple-input static CMOS gates. A method for the reduction of series-connected MOSFETs to a simple MOSFET with the same behavior is proposed. The effective width of the equivalent transistor is not constant as in some previous works. So all cases of input slopes, the load capacitance, the number and the position of the switching inputs, and the body effect, are considered in order to determine the equivalent transistor's width. Along with the reduction process, an accurate analytical inverter timing model is used to compute the propagation delay of multiple-input static gates. The produced results are in very good agreement with SPICE simulations.

WAA15-19 -- A New Curve Fitting Technique For Analysis of Frequency-Dependent Lossy Transmission Lines

Tanji, Yuichi; Nishio, Yoshifumi, and Ushida, Akio, *Tokushima University*

Analysis of frequency-dependent lossy transmission lines is very important for designing the high-speed VLSI, MCM and PCB. The frequency-dependent parameters are always obtained as tabulated data. In this paper, a new curve fitting technique of the tabulating data for the moment

matching technique in interconnect analysis are presented. This method based on Chebyshev interpolation enhances the efficiency of the moment matching technique.

WAA15-20 -- Two-Pole Approximation for High Speed Interconnect Design

Shao, Jianhua and Chen, Richard M. M., *City University of Hong Kong*

In this paper, an approach to find two approximation poles for high speed interconnect design is presented. The approach overcomes the instability problem associated with Pade approximation. These two poles are used for rapid evaluation of line parameter changes. Since transmission line system is a stiff system with some poles of small magnitude and some poles of large magnitude, in general, it is impossible to match the simulated waveform with the calculated waveform using small number of poles. The objective here is to evaluate efficiently the effect of parameter changes in our optimization process. Numerical examples show that the proposed approach can meet our objective.

WAA15-21 -- Analysis of Interconnected Lumped Distributed Multi-Branch Multi-Stage Networks

Sakagami, Iwata, *Muroran Institute of Technology*

Lumped distributed multi-branch networks have been used to model interconnections of logical circuits and computer-networks for the suppression of multiple reflection waves which cause distorted signals. In this paper, a method of deriving network functions(NFs) is discussed by considering the interconnection of three multi-branch networks, because fast output calculations are expected from the analytical NFs. The NFs are confirmed by calculating the frequency characteristics of a broad-band improved hybrid-ring with a multi-stage structure, and also by calculating the step responses of a three-stage network which includes an in homogeneous coupled section.

WAA15-22 -- Precorrected-DCT Techniques for Modeling and Simulation of Substrate Coupling in Mixed-Signal IC's

Costa, Joao Paulo, *INESC / Technical University of Lisbon*; Chou, Mike *Massachusetts Institute of Technology*; Silveira, Luis Miguel, *INESC / Technical University of Lisbon*

Industry trends aimed at integrating higher levels of circuit functionality have triggered a proliferation of mixed analog-digital systems. Magnified noise coupling through the common chip substrate has made the design and verification of such systems an increasingly difficult task. In this paper we present a new method based on a precorrected-DCT algorithm that extends an eigendecomposition-based technique and can be used to accelerate operator application in BEM methods. This method is shown to avoid storage of a dense matrix, as is typical in BEM methods, while at the same time taking all of the substrate boundary effects into account explicitly. This technique can be used for accurate and efficient modeling of substrate coupling effects in mixed-signal integrated circuits.

WAA15-23 -- Analysis of the Transistor Chain Operation in CMOS Gates for Short Channel Devices

Chatzigeorgiou, Alexander and Nikolaidis, Spyridon, *Aristotle University of Thessaloniki*

A detailed analysis of the transistor chain operation in CMOS gates is presented. The chain is diminished to a transistor pair taking into account the actual operating conditions of the structure. The output waveform is obtained analytically, without linear approximations of the output voltage and for ramp inputs. The a-power transistor current model which takes into account second order effects of submicron devices is used, while previous inconsistencies in the chain currents are eliminated by introducing a drain-to-source voltage modulation factor. The exact time when the chain starts conducting is efficiently calculated removing a major source of errors. The calculated output waveform results according to the proposed model are in excellent agreement with SPICE simulations.

WAA15-24 -- Delay and Power Estimation for a CMOS Inverter Driving RC Interconnect Loads

Chatzigeorgiou, Alexander and Nikolaidis, Spyridon, *Aristotle University of Thessaloniki;* and Kyriakis-Bitzaros, Eystathios D., *NCSR "Demokritos"*

The resistive-capacitive behavior of long interconnects which are driven by CMOS gates is analyzed in this paper. The analysis is based on the pi-model of an RC load and is developed for submicron devices. Accurate and analytical expressions for the output voltage waveform, the propagation delay and the short circuit power dissipation are derived by solving the system of differential equations which describe the behavior of the circuit. The effect of the coupling capacitance between input and output and that of short circuit current are also incorporated in the proposed model. The calculated propagation delay and short circuit power dissipation are in very good agreement with SPICE simulations.

WAB6 – DSP Architectures
Chair: Herschel H. Loomis, Jr.
Naval Postgraduate School

11:00am – 12:30pm - ***Room: Ferrante III***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAB6-1 -- General Data-Path Organization of a MAC unit for VLSI Implementation of DSP Processors.

Farooqui, Aamir Alam, *University of California, Davis*, and Oklobdzija, Vojin G., *Integration Berkeley*

This paper describes the data-path and VLSI implementation of a 32x32 bit signed/unsigned multiply accumulate (MAC) unit. In this design we have solved the problem of dealing with signed and unsigned numbers simultaneously, using modified Booth algorithm. This MAC unit can perform 32x32, 32x16, and two 16x16 multiplications, on signed/unsigned operands with a throughput of 2, 1, and 1 cycle, respectively. The Booth encoding technique reduces the number of partial products (PP) by half. Further increase in speed is achieved by using Three Dimensional reduction Method (TDM) to add the partial products. Special circuitry has been designed to accommodate sign/unsigned operands and to deal with sign extension. Modified Booth algorithm coupled with TDM and sign correction circuitry results in a multiplier, with a delay (partial product addition) equivalent to 6 XOR gates. The MAC unit has been modeled in VHDL, and it implements an algorithm which makes this data path organization fast and efficient in silicon.

WAB6-2 -- Nonlinear DSP Coprocessor Cells -- One and Two Cycle Chips

Jain, V.K. and Lin, L., *University of Southern Florida*

Efficient implementation of systolic arrays, and other parallel image processing architectures, has been hindered in the past due to a lack of building blocks, or cells. This paper presents two high-speed floating-point DSP coprocessor cells for rapid computation of nonlinear functions. A new result is produced every two clock cycles for 32 bit Floating-Point arguments and every cycle for 24 bit Fixed-Point arguments in a pipeline mode. This represents an estimated three-to-four fold improvement over other hardware approaches, and a 10 to 20 bold gain over software approaches. The underlying principle which has made the combined goals of high-speed and multi-functionality possible, is second order interpolation of very small ROM tables together with a new innovation, namely "significance-based computation." A 32 bit Floating-Point two-cycle chip for computing the square-root, and a 24 bit Fixed-Point one-cycle ship, both fabricated in 2.0 micron CMOS technology, are presented.

WAB6-3 GAA: A VLSI Genetic Algorithm Accelerator with On-the-Fly Adaptation of Crossover Operators

Wakabayashi, Shin'ichi; Koide, Tetsushi; Hatta, Koichi; Nakayama, Yoshikatsu; Goto, Mutsuaki; and Toshine, Naoyoshi, *Hiroshima Universit*

This paper describes a VLSI implementation of a genetic algorithm, called the Genetic Algorithm Accelerator (GAA) chip. The authors have proposed an adaptive strategy, which selects a crossover operator to be used not in advance but dynamically during the execution of a GA. The GAA chip is a VLSI implementation of a GA with this adaptive strategy for selecting crossover operators. Hardware implementation of GA makes it possible to reduce the computation time drastically. The GAA chip has been designed with the Verilog HDL and simulated with some benchmark functions. According to the simulation, the GAA chip will finish the computation of one generation in less than 0.12ms when the population size is 64. The chip has been fabricated with the CMOS standard cell technology.

WAB6-4 -- VLSI Implementation of a DWT Architecture

Acharya, Tinku, *Intel Corporation*, and Chen, Po-Yueh, *University of Maryland*

In this paper, we presented the VLSI implementation and the simulation results of a systolic architecture for Discrete Wavelet Transform (DWT). This architecture is suitable for both decomposition and reconstruction of signals. The hardware utilization of the architecture is 100% unlike many other existing solution in the literature.

WAB7 – Digital Techniques for Improving Delta-Sigma ADCS Special Session

Chair: Gabor C. Temes
Oregon State University

11:00am – 12:30pm - ***Room: Bonzai I***

*10:30 am – 11:00am – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WAB7-1 -- Some Observations on Tone Behavior in Data Weighted Averaging

Chen, Feng, *Texas Instruments*

Tone behavior of data weighted averaging (DWA)is investigated. Analysis is performed based on system level simulation. In addition, issues of possibly using at low oversampling ratio (<=8) are discussed.

WAB7-2 -- A Reduced-Complexity Mismatch-Shaping DAC For Delta-Sigma Data Converters

Jensen, Henrik, and Galton, Ian, *University of California, San Diego*

Although mismatch-shaping multi-bit DACs offer many advantages over single-bit DACs in delta-sigma shaping DAC architectures involve a large amount of digital processing. This paper presents digital structures that implement previously published tree-structured mismatch-shaping DAC algorithms yet offer significant reductions in the digital processing.

WAB7-3 -- Blind On-Line Digital Calibration of Pipelined Nyquist-Rate and Oversampled A/D Converters

Cauwenberghs, Gert, *Johns Hopkins University*

A linear calibration technique for on-line digital correction of analog imprecisions in the implementation of multi-stage analog-to-digital converters, is presented. The calibration is `blind', in that it uses no reference and operates directly on the digital output during conversion. The only assumption made on the input signal is that its spectrum is bandlimited. The excess sampling over Nyquist bandwidth is used for least-squares auto-zeroing calibration. The technique extends directly to digital correction of multi-stage oversampled A/D converters where a multi-bit quantizer is implemented using a pipelined algorithmic A/D converter. Behavioral simulations on pipelined algorithmic and dual-quantization oversampled A/D converters demonstrate significant improvements in signal-to-quantization-noise performance over the uncalibrated case.

WEDNESDAY AFTERNOON -- JUNE 3, 1998

WPA1-Wavelets: Implementation and Application

Chair: Truong Nguyen
Boston University

2:00pm – 5:30pm - ***Room: Colton I***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA1-1 -- Nonstationary Signal Classification Using Pseudo Power Signatures

Venkatachalam, Vidya, and Aravena, Jorge L., *Louisiana State University*

This paper deals with the problem of classification of nonstationary signals using signatures which are essentially independent of the signal length. We develop the notion of a separable approximation to the Continuous Wavelet Transform (CWT) and use it to define a power signature. We present a simple technique which uses the Singular Value Decomposition (SVD) to compute such an approximation, and demonstrate through an example how it is used to perform the classification process. This example serves to show both the effectiveness and the limitations of the approach. Our main result is an alternate approach which develops the idea of using orthogonal projections to refine the approximation process, thus allowing for the definition of better signatures.

WPA1-2 -- A Simple Scheme of Decomposition and Reconstruction of Continuous-time Signals by B-splines

Ichige, Koichi. *University of Tsukuba;* Kamada, Masaru, *Ibaraki University*; and Ishii, Rokuya, *Yokohama National University*

An approximate scheme is proposed for decomposing and reconstructing a continuous-time signal as a linear combination of the B-splines. It is an oversampling discrete-time implementation derived by substituting the multifold RRS functions for the B-splines. Its analysis yields conditions for the circuit parameters to avoid instability and overflow, and to meet required precision. A design example and its numerical simulation are also presented.

WPA1-3 -- A VLSI Architechture Design with Lower Hardware Cost and Less Memory for Separable 2-D Discrete Wavelet Transform

Sheu, Ming-Hwa; Shieh, Ming-Der; and Liu, Sheng-Wel, *National Yunlin University of Science and Technology*

*This paper presents and efficient architecture for 2-D image decomposition of discrete wavelet transform. Our design approach reduces the transpose storage size and hardware cost efficiently, based on the input data reuse methodology and fully parallel pipelined architecture. The main characterisitcs of the architecture include: (1) lower hardware costs; (2) smaller transpose storage size, (3) shorter latency; (4) suitable VLSI implementation. Finally, all components in our architecture are simulated based on the accuracy requirement and realized as a simgle chip physically. The chip area is about 7600*8400mm2 and its working frequency is 25 MHz.*

WPA1-4 -- Synthesis Filter Bank With Low Memory Requirements For Image Subband Coding

Sundsbo, Ingil, *Nordic VLSI ASA;* and Ramstad, Tor A., *Norwegian University of Science and Technology*

One of the factors that makes subband coding seem less attractive for image processing compared to transform coding, is the extensive memory requirements for 2-D filtering. In this paper we present a filtering method that significantly lowers the memory requirements. A parallel, uniform and separable filter bank with 8 channels in each dimension is considered. It is shown that by a data reordering and a minor structural change to the filter bank, a blockwise filtering is made possible, thus reducing the total memory to 192 B registers and 9 dB RAM for an image of size 1152 x 1920 pixels.

WPA1-5 -- Optimal Design of Interpolating Wavelet Transform

Shui, PengLang, *XiDian University*

In this paper, we investigate the properties of an Interpolating Wavelet and present optimal design criteria along with a local orthogonalization optimal algorithm to reduce redundancy. We can find that the obtained optimal wavelet system performs better in compressing real data compared to the original system.

WPA1-6 -- Semi-recursive VLSI Architecture for Two-dimensional Discrete Wavelet Transform

Paek, Seung-Kwon, *Korea Advanced Institute of Science and Technology*

This paper presents an efficient two-dimensional discrete wavelet transform (2-D DWT) VLSI architecture which calculates the 2-D DWT for image processing in real-time. The proposed architecture, Semi-recursive 2-D DWT VLSI architecture, has the minimum H/W cost of internal word length, data-bus utilization, scheduling control overhead, and storage size. Compared with the conventional recursive 2-D DWT VLSI architecture, the size of multipliers and registers are reduced by the amount of 13% and 34%. Furthermore, the semi-recursive 2-D DWT VLSI architecture exploits the lapped block processing and hence has the minimum transposition storage size and the short latency.

WPA1-7 -- Implementation of 2-D Wavelet Transform on TESH connected Parallel Processors

Maziarz, Bogdan M., and Jain, Vijay K., *University of South Florida*

This paper presents the mapping of the 2-D wavelet transform onto a TESH connected multi-processor system. TESH (Tori connected mESHes) is a recently developed interconnection network. Key features of the network are the following: it is hierarchical, thus allowing exploitation of computation locality as well as easy expansion up to a million processors, it permits efficient VLSI/ULSI realization, and appears to be well suited for 3-D VLSI/ULSI implementation. Specifically, the paper develops a parallel algorithm implementation on TESH network, in such a way so as to completely hide the communication overhead. Correspondingly, the system performance is evaluated both for the TESH and for the familiar MESH. It is shown that the performance of a TESH implemented algorithm is comparable to the MESH based algorithm. However, large TESH networks are easier to implement because of the significantly reduced bisection width than large MESH networks.

WPA1-8 -- Polyphase Adaptive Filter Banks for Subband Decomposition

Gerek, Omer Nezih, and Cetin, A. Enis, *Bilkent University*

Subband decomposition is widely used in signal processing applications including image and speech compression. In most practical cases, the goal is to obtain subband signals that are suitable for data compression. In this paper, we present Perfect Reconstruction (PR) polyphase filter bank structures in which the filters adapt to the changing input conditions. This leads to higher compression results for images containing sharp edges, text, and subtitles.

WPA2-3D Data Modeling and Imaging — Special Session

Chair: Guido Cortelazzo

University of Padova

2:00pm – 5:30pm - ***Room: Colton II***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA2-1 -- Hybrid Modeling for Manufacturing using NURBS, Polygons, and 3D Scanner Data

Besl, Paul J., *Alias Wavefront, Inc.*

Some systems provide 2D environments where users can (1) import imagery from 2D cameras, (2) create new geometry and imagery, (3) combine the imported with the new, and (4) create high-quality production output. In contrast, most 3D modeling systems provide either NURBS or polygonal modeling with no import options from 3D cameras. 3D cameras/scanners are used efficiently today to create polygonal models, but high-quality NURBS modeling from 3D scanner data remains difficult and time-consuming. Ideally, designers could focus on 3D geometry and application issues in a manner independent of internal representations. It should be possible to import from any 3D geometry source, create 3D geometry, and freely intermix various types of shape information to create 3D models of sufficient quality that they can be manufactured with at least the ease of existing NURBS modeling systems. This paper discusses some of the issues involved in such a system.

WPA2-2 -- Portable Digital 3-D Imaging System for Remote Sites

Beraldin, J-Angelo, *National Research Council Canada*

A portable digital 3D imaging system based on laser triangulation was designed for the accurate documentation of environments and objects located in remote sites. Cultural heritage and industrial applications are among the best candidates to benefit from this new technology. This paper focuses on such aspects as the acquisition, display, calibration/verification, and especially on model building. These aspects were all optimized to create a versatile system that is truly portable, i.e. hand portable to a remote site. Emphasis is placed on accuracy verification and monitoring which are critical factors for obtaining high-quality reconstruction of 3D models from multiple range images. A summary of the experimental results acquired at a number of sites in Italy is presented in this paper.

WPA2-3 -- 3D Photography Using Shadows

Bouguet. Jean-Yves and Perona, Pietro, *California Institute of Technology*

A simple and inexpensive approach for extracting the three-dimensional shape of objects is presented. It is based on `weak structured lighting;' it differs from previous structured lighting approaches in that it requires little hardware besides the camera: a light source (a desk-lamp or the sun), a stick and a checkerboard. The object, illuminated by the light source, is placed on a stage composed of a ground plane and a back plane; the camera faces the object. The user moves the stick in front of the light source, casting a moving shadow on the scene. The 3D shape of the object is extracted from the spatial and temporal location of the observed shadow. Experimental results are presented on three different scenes (indoor with a desk lamp and outdoor with the sun) demonstrating that the error in reconstructing the surface is less than 0.5% of the size of the object.

WPA2-4 -- View-Dependent Texture Coding Using the MPEG-4 Video Coding Scheme

Jordan, Fred D.; Ebrahimi, Touradj; and Kunt, Murat, *EPFL - LTS*

We present a novel technique for efficient coding of texture to be mapped on 3D landscapes. It enables the streaming of texture information across bi-directional networks like the internet. The algorithm can be used with many transform based coding schemes. Results are presented using MPEG-4 video encoder.

WPA2-5 -- Systems for Disparity-Based Multiple-View Interpolation

Ohm, Jens-Rainer, Izquierdo, Ebroul, and Muller, Karsten, *Heinrich-Hertz-Institut*

Viewpoint adaptation from multiple-viewpoint video captures is an important tool for telepresence illusion in stereoscopic presentation of natural scenes, and for the integration of real-world video objects into virtual 3D worlds. This paper describes different low-complexity approaches for generati9on of virtual-viewpoint camera signals, which are based on disparity-processing techniques and can hence be implemented with much lower complexity than full 3D analysis of natural objects or scenes. A realtime hardware system, which is based on one of our algorithms, has already been developed.

WPA2-6 -- 2-D Patterns for 3-D Surface Matching

Johnson, Andrew Edie, *Jet Propulsion Laboratory*

Surface matching is the process that compares the shape of two surfaces. To facilitate surface matching, we have developed a 2-D representation for comparing 3-D surfaces of arbitrary shape. Using a cylindrical mapping, a descriptive pose-invariant 2-D pattern is created for every point on the surface of an object. By comparing patterns, point correspondences between different surfaces are established. When a sufficient number of point correspondences exist between two surfaces, the surfaces match. We show that the simplicity and generality of our representation makes it widely applicable to problems in 3-d computer vision including object modeling, interior modeling and object recognition.

WPA2-7 -- Review of Methods for Object-Based Coding of Stereoscopic and 3D Image Sequences

Strintzis, Michael G., *University of Thessaloniki*

Object-based coding of stereo sequences is a promising alternative to block-based schemes, since not only produces fewer coding artifacts but also provides a structural description of the scene useful in many applications. In this paper we review techniques for the object coding of stereoscopic video. The basic structure common to most of the object based techniques in the literature is described. The advantages and

shortcomings of these schemes are also discussed. Application of object-based coding to the communication of multi-view image sequences and 3Ddata is finally presented.

WPA2-8 -- Image-based Modeling and Rendering of Architecture with Interactive Photogrammetry and View-Dependent Texture Mapping

Debevec, Paul Ernest, *University of California at Berkeley*

In this paper we overview an approach to modeling and rendering architectural scenes from a sparse set of photographs. The approach is designed to require no special hardware and to produce real-time renderings on standard graphics hardware. The modeling method is an interactive photogrammetric modeling tool for recovering geometric models of architectural scenes from photographs. The tool is practical as an interactive method because it solves directly for architectural dimensions rather than for a multitude of vertex coordinates or depth measurements. The technique also determines the camera positions of the photographs, allowing the photographs to be taken from arbitrary unrecorded locations. The rendering method creates novel views of the scene based on the recovered model and the original photographs. A view-dependent texture mapping method allows all available image information to be used to produce the most photorealistic renderings. We focus on a number of results and applications of the method.

WPA2-9 -- A Frequency Domain Method for Registration of Range Data

Cortelazzo, G.M., Doretto, G., Lucchese, L., and Totaro S.
University of Padova

Free-form 3-D surfaces registration is a fundamental problem in 3-D imaging, typically approached by extensions or variations of the ICP algorithm. This work presents an alternative method for 3-D motion estimation based on the Fourier transform of the range data. The frequency domain techniques for estimating motion parameters are non feature-based methods suitable for unsupervised registration of 3-D view. The proposed method can give unsupervised registration of range data within 1° of accuracy of the angular parameters, useful "per se" in applications where this kind of precisions is adequate or which can serve as good starting point for the ICP algorithm when a higher precision is needed.

WPA3 –Cellular Neural Networks

Chair: Jacek M. Zurada
University of Louisville

2:00pm – 5:30pm - ***Room: Colton III***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA3-1 -- A Modular gmC Programmable CNN Implementation

Lím, Drahoslav; and Moschytz, George S., *Swiss Federal Institute of Technology*

A programmable cellular neural network has been designed in a 0.8 micron CMOS technology. An arbitrarily large analog CNN can be constructed by modularly connecting `tile' CNN chips, each with a modest number of cells. The network operates in continuous time, has a PWL output function, and the cell connections (template values) are realized as sets of switchable unit and half-unit transconductors. Matching accuracy, including matching among chips from different manufacturing runs, and operation was verified on uncoupled and coupled templates.

WPA3-2 -- An Improved Architecture for the Interconnections in a Multi-Chip CNN System

Sargeni, Fausto; Sorgeni, Fausto; and Bonaiuto, Vincenzo, *University of Rome "Tor Vergata"*

The design and realisation of high number of cells reliable hardware CNN systems is a key point in researching on this field. In fact, several different solutions have been proposed in these years in VLSI implementations. In previously published papers, the authors presented a current-mode interconnection-oriented integrated circuits to carry out a wide CNN network. The multi-chip architecture shows the drawback to be a pad-limited structure because of the growing number of the pads required by the interconnections. In this paper a technique to improve the interconnection architecture without any lack of functionality will be presented. This approach will drastically cut off the interconnections requirements of 75%. Some simulation results will be presented together with experimental results.

WPA3-3 -- VLSI Delta-Sigma Cellular Neural Network for Analog Random Vector Generation

Cauwenberghs, Gert, *Johns Hopkins University*

We present a cellular neural network architecture for parallel analog random vector generation, including experimental results from an analog VLSI prototype with 64 channels. Nearest-neighbor coupling between cells produces parallel channels of uniformly distributed random analog values, with statistics that are truly uncorrelated across channels and over time. The cell for each random channel emulates an integrating nonlinearity essentially implementing a delta-sigma modulator, and measures 100umX120um in 2um CMOS technology. Applications include analog encryption and secure communications, analog built-in self-test, stochastic neural networks, and simulated annealing optimization and learning.

WPA3-4 -- On Evolving Hardware: On-Line Evolution by Cellular Programming

Nicoletti, Guy M., *University of Pittsburgh at Greensburg*

Extensive research shows that the implementation of evolutionary algorithms are costly in many cases. [1]. This paper reports on an alternative construct, namely non-uniform cellular automatons (CA) with which (1) it is possible to increase the capacity for complex computations while preserving the main features of CAs, (2) evolve parallel cellular machines to perform computational tasks via cellular programming, and (3) attain evolware with implementations centering on hardware. The hardware architecture on the cellular programming evolware departs from [1] in that: (1) a group of individual cells is in operation rather than a single one, (2) genetic operators are implemented on-board rather than on offline computer, and (3) the evolutionary phase proceeds uninterrupted via a continuous machine's operation. The active components of the evolware complex comprise exclusively the latest cellular FPGA circuit. Accordingly, this paper is organized as follows: Section I presents fundamentals and analysis of computations in Quasi-Uniform Cellular Automata in a quasi-uniform cellular space. Section II introduces the basic approach for Coevolving Cellular Computation and Cellular Machines, denoted Cellular Programming [2]. Section III adopts synchronization as a criteria to attain evolware centered on hardware. Cellular programming is implemented in hardware. The algorithm is slightly modified (without loss of performance): the genetic operators, one-point crossover and mutation, are replaced with the operator uniform crossover. This results in the creation of an offspring genome from two parent genomes (bit strings) with a 50% probability for each parent. Finally, Section IV analyzes performance and results.

WPA3-5 -- An Analysis of CNN Settling Time

Moschytz, George S and Haenggi, Martin;*Swiss Federal Institute of Technology*

The settling time of cellular neural networks (CNNs) is crucial for both simulation and applications of VLSI CNN chips. The computational effort for the numerical integration may be drastically reduced, and CNN programs can be optimized, if a priori knowledge on the settling time is available. Moreover, this allows the parameters necessary to achieve higher processing speed to be tuned. For certain template classes, we present analytic solutions, while for others, tight upper bounds are given.

WPA3-6 -- Learning Algorithms for Cellular Neural Networks

Mirzai, Bahram;and Moschytz, George S., *Swiss Federal Institute of Technology*

A learning algorithm based on the decomposition of the A-template into symmetric and anti-symmetric parts is introduced. The performance of the algorithm is investigated in particular for coupled CNNs exhibiting diffusion-like and propagating behavior.

WPA3-7 -- Autowaves for Motion Control: A CNN Approach

Arena, Paolo; Fortuna, Luigi; Branciforte, Marco; and Di Grazia, Pietro *Università degli Studi di Catania;*

In this paper the CNN paradigm is used for the first time to generate and control motion in mechatronic devices. In particular it is shown that autowaves, commonly met in living systems, can be used as the basis to generate and control motion in some devices built strictly reflecting architectural paradigms met in animals belonging to the earlier rings in the evolution chain. Such a strategy offers an interesting starting point for the design of biologically inspired walking robots.

WPA4 – High Level Synthesis

Chair: Forrest D. Brewer

University of California at Santa Barabara

2:00pm – 3:30pm - Room: Ferrante I

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA4-1 -- Parallel Algorithms for Simultaneous Scheduling, Binding and Floorplanning in High-level Synthesis

Banerjee, Prithviraj, *Northwestern University* and Prabhakaran, Pradeep Kumar, *University of Illinois, Urbana Champaign*

With small device features in sub-micron technologies, interconnection delays play a dominant part in cycle time. Hence, it is important to consider the impact of physical design during high level synthesis. In comparison to a traditional approach which separates high-level synthesis from physical design, an algorithm which is able to make these stages interact very closely, would result in solutions with lower latency and area.

However, such an approach could result in increased runtimes. Parallel processing is an attractive way of reducing the runtimes. In this paper, two parallel algorithms for simultaneous scheduling, binding and floorplanning algorithm are presented. A detailed hardware model is considered, taking into account multiplexor and register areas and delays. Experimental results are reported on an IBM SP-2 multicomputer, with close to linear speedups for a set of benchmark circuits.

WPA4-2 -- A Simple Alternative for Storage Allocation in High-level Synthesis

Aloqeely, Mohammed A., *King Saud University*

A recent trend in high-level synthesis is to introduce special structure memory elements as an alternative to RAMs which suffer from address generation and decoding overhead. In this paper, an alternative, called Sequential FIFO Memory (SFM) is investigated. The problem of allocating variables to SFMs is studied thoroughly including the theoretical background, mapping algorithms and experiments. Moreover, the combinatorial optimization problems related to SFMs were found to be tractable in contrast to those of previous non-RAM alternatives.

WPA4-3 -- A New Partitioning Framework for Uniform Clock Distribution During High-Level Synthesis

Krishnamurthy, Harsha, *Intel Corp.*; and Maaz, Mohamad and Bayoumi, Magdy, *The University of Southwestern Louisiana*

In this paper, we present a new partitioning framework that significantly provides uniform clock distribution during high-level synthesis. This weighted cluster partitioning technique is aided by an innovative resource allocation technique which provides a uniform resource utilization. This results in a uniform power requirement distribution across the synthesized chip which is practically beneficial as well. The resource cluster information obtained from this new partitioning synthesis framework could be used to aid the hierarchical placement and routing tools as well as the clock-router to design and produce a close to optimal uniform clock routing. This new framework applies the idea of local (intra-cluster) communication, while minimizing global communication busses. This resulted in a low power design as well. The partitioner cost function considers three factors: the number of clock lines per unit area, the number of cuts between clusters, and the size of partitions. Experimental results show that this partitioning framework provides uniform clock distribution among clusters as well as fairly uniform sized partition

WPA4-4 -- A Binding Algorithm for Retargetable Compilation to Non-Orthogonal Datapath Architectures

Masayuki, Yamaguchi, *SHARP Corporation*; Nagisa, Ishiura, *Osaka University*; Takashi, Kambe, *SHARP Corporation*

This paper presents a new binding algorithm for a retargetable compiler which can deal with diverse architectures of application specific embedded processors. The architectural diversity includes a ``non-orthogonal'' datapath configuration where all the registers are not equally accessible by all the functional units. Under this assumption, binding becomes a hard task because inadvertent assignment of an operation to a functional unit may rule out possible assignment of other operations due to unreachability among datapath resources. We propose a new BDD-based binding algorithm to solve this problem. In the experiments, a feasible binding which satisfies the reachability is found or the deficiency of datapath is detected within a few seconds.

WPA5 – Archs., Algors., and Impl. for Wireless Communications Systems

Chair: H. V. Poor

Princeton University **Special Session**

Organizers: *H. V. Poor*

Princeton University
G. W. Wornell
MIT

2:00pm – 5:30pm - ***Room: Ferrante II***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA5-1 -- Creating and Exploiting Diversity in Wireless Systems: A Signal Processing Perspective

Wornell, Gregory W., *Massachusetts Institute of Technology*

Diversity techniques have a critical role to play in counteracting the effects of signal-to-noise ratio variation due to multipath-propagation in wireless communication systems. We give an overview of some key ways in which computationally efficient signal processing algorithms can be used at the transmitters and receivers of multiuser communication systems to realize effective forms of diversity. Such diversity is achieved by, in effect, spreading the transmission of symbols spectrally, temporally, and/or spatially to within the limits imposed by bandwidth, delay, and other physical system constraints. We discuss how both recently introduced spread-signature CDMA protocols and suitably designed multiple-element

transmitter antenna arrays can be used to realize spreading of this type. All such techniques have the characteristic that they improve both average and worst-case performance, and can be used in conjunction with---or as an alternative to---coding in such systems.

WPA5-2 -- Blind Demodulation Of High-Order QAM Signals In The Presence Of Cross-Pole Interference

Treichler, John and Bohanon, Jon, *Applied Signal Technology, Inc.*

Technology has been developed over the past decade to permit the blind demodulation of high-order QAM signals in the presence of time-varying dispersion introduced by the propagation channel between the transmitter and the receiver. This technology has been recently extended to address the problem of blind demodulation in the face of interference from a cross-polarized signal. This paper describes the "cross-pole" interference problem and high-lights the design of a practical demodulator built to solve it.

WPA5-3 -- Signal Processing Algorithms for Adaptive Interference Suppression

Poor, H. Vincent, *Princeton University*

Future wireless communication systems will involve significant adaptive signal processing capabilities to enhance the performance of high-rate transmission through limited-bandwidth, dynamic multiple-access channels. Structured interference is a dominant, performance-limiting characteristic of such channels, and this paper provides a brief overview of basic adaptive signal processing algorithms that are useful for combatting this problem. This overview focuses primarily on adaptive linear methods for the suppression of multiple-access interference, although the mitigation of such impairments as dispersion and impulsive noise, and the exploitation of receiver diversity arising either from natural multipath or from the use of multiple antennas, are also discussed briefly. The discussion considers algorithms based on traditional techniques such as recursive-least-squares, as well as those based on more recently developed methods involving subspace tracking.

WPA5-4 -- Design of a Wideband Spread Spectrum Radio Using Adaptive Multiuser Detection

Teuscher, Craig, Yee, Dennis, Zhang, Ning and Brodersen, Robert, *UC Berkeley*

This paper describes the design of a wideband spread spectrum radio using adaptive multiuser detection in an indoor wireless environment. System specifications are provided, and the feasibility of an integrated CMOS receiver implementation is discussed. The proposed receiver architecture uses a wideband analog front-end to reject out-of-band interference, and multiuser detection in the digital baseband to suppress interference from other system users.

WPA5-5 -- Distributed Network Protocols for Wireless Communication

Meng, Teresa H. and Rodoplu, Volkan, *Stanford University*

This paper describes a network design strategy that focuses on energy conservation. This position-based network protocol is optimized for minimum energy consumption in wireless networks that support peer-to-peer communications. Given any number of randomly deployed communication nodes over an area, we show that a simple local optimization scheme executed at each node guarantees strong connectivity of the entire network and attains the global minimum energy solution.

WPA5-6 -- Trends in Low Power Digital Signal Processing

Meng, Teresa H. and Rodoplu, Volkan, *Stanford University*

System level optimization will be required for the implementation of ultra low power portable devices. Often, system properties such as data distribution or network configuration can be exploited to minimize computational switching. Embedded power supply systems configured in performance feedback also minimize energy dissipation under varying temperature, process parameters and computational workload. If the power dissipation of digital processors can be scaled to low enough levels, self-powered techniques can be used to achieve "infinite" lifetime and low-maintenance wireless operation.

WPA5-7A 1 -- V Programmable DSP for Wireless Applications

Lee, Wai, Landman, Paul, Barton, Brock, Frantz, Gene; *Texas Instruments*

To address the need for low power base-band signal processing in future portable wireless devices, an energy-efficient, programmable DSP chip that operates from a 1 V supply has been designed, fabricated, and tested. This DSP chip incorporates a number of architectural, circuit, and process features that enable 60 MHz operation at 1 V with a power dissipation of only 17 mW.

WPA5-8 -- Low-Power Radio Frequency Circuit Architectures for Portable Wireless Communications

Larson, Lawrence E., *University of California - San Diego*

Next generation portable wireless communications devices will require improved architectures and circuit design techniques in the radio frequency portion of the transceiver. This talk will summarize some of the most promising recent developments in the field, with particular attention to power amplifier design and transceiver architectures.

WPA6 – Topics in Analog and Digital Test
Chair: Ramesh Harjani
University of Minnesota

2:00pm – 5:30pm - ***Room: Ferrante III***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA6-1 -- Low Expense Architectures for a Dynamic Spectrum Analyzer Based on SC-Filters

Marschner, Uwe; Fischer, Wolf-Joachim; and Kranz, Ernst-Georg, *Dresden University of Technology*

In this contribution new architectures for a dynamic spectrum analyzer are presented. The basis of the spectrum analyzer is a Switched Capacitor (SC-) filter which is periodically reprogrammed or tuned by a change of the clock frequency. For a small reprogramming cycle time a hyperbolic change of the clock frequency is applied. In the first part of the paper the effects of a stepwise and continuous reprogramming are investigated. In the second part analog and digital hyperbolic clock generators are presented.

WPA6-2 -- A Multi-Pass A/D Conversion Technique For Extracting On-Chip Analog Signals

Hajjar, Ara and Roberts, Gordon W., *McGill University*

A high speed and area-efficient A/D convertor is proposed for mixed-signal test applications. Only a single on-chip comparator is required to digitize repetitive analog waveforms. Simulations show 10 bits of amplitude resolution at 300 MHz for a bipolar comparator design (0.8um BiCMOS process), and 10 bits of amplitude resolution at 667 MHz for a CMOS comparator design (0.5um CMOS process).

WPA6-3 -- Arbitrary Band-Limited Pulse Generation for Built-In Self-Test Applications

Dufort, Benoit and Roberts, Gordon W., *McGill University*

This paper describes a new technique to generate a variety of arbitrary band-limited pulse shapes that can be used efficiently in built-in self-test applications. The proposed method requires very little area and the same hardware can be used to generate pulses of different shapes. This is particularly useful in testing receivers with different pulse shapes coming from the transmission medium such as a twisted pair cable. Experimental results from an on-chip CMOS generator will also be given.

WPA6-4 -- An Effective BIST Scheme for Delay Testing

Li, Xiaowei and Cheung, Paul Y.S., *The University of Hong Kong*

This paper presents a BIST scheme for the detection of path delay faults. It differs from the traditional BIST schemes which aim at stuck-at faults by offering higher capability of two-pattern generation. The TPG scheme produces test sequences having exactly the same robust path delay fault coverage as single-input-change test sequences. By determining non-adjacent inputs, the reduction of both test length and area overhead can be achieved. Signature analysis under path delay fault is also discussed. Based on true-value simulation, error patterns under path delay fault model were obtained and were used in aliasing estimation.

WPA6-5 -- Design of Single-Ended SRAM with High Test Coverage and Short Test Time

Wu, Chi-Feng; Wang, Chua-Chin; Hwang, Rain-Ted; and Kao, Chia-Hsiung, *National Sun Yat-Sen University*

The advantages of low power dissipation and smaller chip area for single-ened SRAM are well known. In this paper we present the configuration and the test strategy of a single-ended six-transistor SRAM. The benefits of short test time, no retention test and high test coverage are verified. The goal of high quality control and short test time of full CMOS SRAM test can be achieved.

WPA6-6 -- Reducing Power Consumption During Test Application by Test Vector Ordering

Girard, Patrick; Landrault, C.; Pravossoudovitch, S.; and Severac, P.; *Université Montpellier II/CNPS*

This paper considers the problem of testing VLSI integrated circuits without exceeding their power ratings during test. The proposed approach is based on a re-ordering of the vectors in the test sequence to minimize the switching activity of the circuit during test application. Our technique uses the Hamming distance between test vectors and guarantees a decrease in power consumption and heat dissipation without modifying the initial fault coverage. Results of experiments are presented at the end of this paper, and shows a reduction of the circuit activity in the range from 8.2 to 54.1 % during test application.

WPA6-7 -- A Simplicial Method for the Simulation of Transistor Shorts in CMOS Logic Gates

Lin, Hung-Jen and Milor, Linda, *University of Maryland at College Park*

CMOS logic gates in the presence of gate-to-drain or gate-to-source shorts generally depend on electrical-level simulators such as SPICE to predict the circuit behavior which is required for the purpose of fault simulation. In the light of a wide variety of unintended networks caused by transistor shorts, the use of SPICE can be very computationally intensive. In this paper, a simplicial technique for characterizing the static responses of faulty CMOS gates is presented. Example circuits are used to demonstrate the feasibility of the method. The results indicate that computational time can be reduced by a factor of 10 to 100 in comparison to SPICE simulation.

WPA6-8 -- Artificial Neural Network Based Multiple Fault Diagnosis In Digital Circuits

Al-Jumah, Abdullah A. and Arslan, T., *Cardiff University of Wales*

The paper describes a technique, based on the use of Artificial Neural Networks (ANNs), for the diagnosis of multiple faults in digital circuits. The technique utilizes different quantities of randomly selected circuit test data derived from a fault truth table which is constructed by inserting random single stuck-at faults in the circuit. The paper describes the diagnostic procedure using the technique, the ANN architecture and results obtained with example circuits. Our results demonstrate that when the test data selection procedure is guided by test vectors of the circuit a compact, efficient and flexible ANN architecture is achieved.

WPA7 – Controlling Bifurcations and Chaos **Special Session**
Chair: Guanrong Chen
University of Houston
Organizers: Guanrong Chen
University of Houston
Wei Kang
Naval Postgraduate School
Hua O. Wang
Duke University

2:00pm – 5:30pm - ***Room: Bonzai I***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA7-1 -- Predicting Period-Doubling Bifurcations in Nonlinear Time-Delayed Feedback Systems

Berns, Daniel W., *Universidad Nacional de la Patagonia San Juan Bosco*
Moiola, Jorge L., *Universidad Nacional del Sur*; Chen, Guanrong *University of Houston*

A graphical approach is developed in this paper for detecting the period-doubling bifurcation emerging near the Hopf bifurcation point of a time-delayed feedback system. The new algorithm employs higher-order harmonic balance approximations (HBAs) for estimating the predicted periodic solutions of the system. Prediction of the period-doubling bifurcation is accomplished using a type of distortion index based on some information about the higher-order harmonics. The time-delayed Chua's circuit is used as an example for illustration.

WPA7-2 -- Rotating Stall Control Via Bifurcation Stabilization

Chen, Xiang; Gu Guoxiang,; Martin, Phillip B.; and Zhou Kemin, *Louisiana State Universit*

Rotating stall is a fundamental aerodynamic instability in axial flow compressors, induced by nonlinear bifurcation. It significantly reduces the performance of aeroengines. In this paper classical bifurcation theory is used to derive output feedback control laws in which throttle position is employed as actuator and pressure rise as output measurement. The challenge to the proposed control system is that the critical mode of the linearized system corresponding to rotating stall is neither controllable nor observable. Using the projection method, it is shown that the proposed control system is effective for elimination of rotating stall for the 3rd order Moore-Greitzer model.

WPA7-4 -- Bifurcation Analysis and Control of Nonlinear Systems with a Nonsemisimple Zero at Criticality and Application

Fu, Jyun-Horng (Alex), *Systems Planning and Analysis Inc.*

Bifurcation analysis and control for nonlinear systems with a defective repetitive zero at criticality is presented. The results are applied to stabilization of a flexible, inverted pendulum mounted on a moving cart which is approximated with a coefficient of flexibility.

WPA7-5 -- Stabilization of a Class of Bifurcations via State Feedback

Fitch, Osa *NAVAIR* and Kang, Wei, *Naval Postgraduate School*

This paper presents a general method for the control or stabilization of the class of local bifurcations commonly occurring in engineering systems, such as saddle-node, transcritical, pitchfork and Hopf bifurcations. The method presented shows that the problem can be solved by transforming the system into its quadratic normal form, a simplified system with equivalent dynamics, and then examining the resulting dynamics on the center manifold of the system. The dynamics on the center manifold can then be altered by linear and quadratic state feedback of the center states. The feedback gains required are given by simple algebraic combinations of the coefficients of the quadratic normal form..

WPA7-6 -- Suppressing Cardiac Alternans: Analysis and Control of a Border-Collision Bifurcation in a Cardiac Conduction Model

Chen, Dong and Wang, Hua O., *Duke University*; and Chin, Wai, *Colorado State University*

This paper describes the utility of dynamic bifurcation control for suppressing a pathological period-2 rhythm (cardiac alternans) in an atrioventricular modal conduction model. A commonly held view has linked alternans rhythms in this model to period-doubling bifurcations. Our analysis shows that the alternans rhythm is actually associated with a period-1 to period-2 border-collision bifurcation. In the control design, we employ a dynamic feedback control incorporating washout filter to suppress the cardiac alternans. Important features of the dynamic control law include equilibrium preservation even in the presence of model uncertainty, and automatic targeting of the orbits to be controlled. An independent experiment of suppressing cardiac alternans in a piece of dissected rabbit heart demonstrates the viability and utility of the proposed bifurcation control approach. Controlling nonlinear cardiac dynamics may have important clinical implications since arrhythmias in the heart such as fibrillation and ectopic foci are life threatening. The controller designs described here can lead to the development of future smart clinical pacemakers.

WPA7-7 -- Feedback Control of Hopf Bifurcations

Chen, Guanrong; Yap, Keng C.; and Lu, Jialiang, *University of Houston*

Bifurcation control has attracted increasing attention in recent years. A simple and unified state-feedback methodology is developed in this paper for Hopf bifurcation controls for both continuous-time and discrete-time systems. The control task can be either shifting an existing bifurcation or creating a new one. Some computer simulations are included to illustrate the methodology and verify the theoretical results.

WPA8 – Current Mode Techniques
Chair: Arash Loloee
Texas Instruments

2:00pm – 5:30pm - ***Room: Bonzai II***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA8-1 -- A 50th Order Elliptic LP-Filter Using Current Mode Gm-C Topology

Kosunen, Marko, Koli, Kimmo, and Halonen, Kari, *Helsinki University of Technology*

A 50 Mhz 5th order elliptic LP-filter with current mode Gm-C topology has been designed for 0.5um CMOS process and 3.3 V supply voltage. A low distortion level has been achieved by using dynamic biasing as a linearization principle. In order to further reduce the level of distortion, scaling for minimum distortion has been done. The effect of poles caused by parasitic capacitances has been canceled with phase lag compensation resistances realized with transistors biased in the saturation region in order to achieve high adjustability. With this topology the level of third order harmonic approximately 55 dBc with 500App input current has been achieved. The simulated dynamic range of the filter is 57 dB and it has power dissipation of 91 mW.

WPA8-2 -- A Low Mismatch Sensitivity Fully-Balanced Current-mode Integrator

Sanchez-Sinencio, Edgar, *Texas A&M Univ*

An improved fully-balanced current-mode integrator structure is presented. The proposed structure improves the low frequency CMRR of integrators reported in the literature from the order of g_{m}/g_{o} to g_{m}^2/g_{o}^2. Moreover, the new structure provides more flexibility to guarantee stability and is less sensitive to process mismatch. Several integrator topologies are compared. The differential and common-mode gains and the CMRR at low and high frequencies are analyzed.

WPA8-3 -- A CMOS current-mode multiplier/divider circuit.

Baturone, Iluminada, *Instituto de Microelectronica deSevilla (IMSE-CNM*

Combination of A/D-D/A converters allows implementing multiplier/divider operations. An efficient design based on continuous-time, current-mode, dividing-algorithmic converters is presented in this paper. It offers high speed and capability of low voltage operation, and it is suitable for applications of low or middle resolution (below 9 bits). In addition, the division result is given in both analog and digital formats. Experimental results from a CMOS prototype with 5 bit resolution are included.

WPA8-4 -- Sampling Jitter in High-Speed SI Circuits

Jonsson, Bengt E., *Ericsson Radio Systems AB*

Random and signal dependent sampling time uncertainty in high-speed switched-current circuits are analyzed, and a comparison with voltage-mode sampling is made. The similarity of the two techniques is shown as well as the fact that the lower voltage swing in switched-current circuits, makes them less sensitive to the signal dependent switch-off time of the sampling switch. Derivations and simulation results showing the effects of clock phase-noise, additive clock driver noise, and signal-dependent sampling time uncertainty are included. Reduction of signal-dependent jitter errors by using fully-differential switched-current sampling is also illustrated.

WPA8-5 -- The Multiple-Input Translinear Element: A Versatile Circuit Element

Minch, Bradley A., *Cornell University*, and Hasler, Paul, *Georgia Institute of Technology* and Diorio, Chris, *University of Washington*

We define the multiple-input translinear element (MITE), a versatile circuit primitive from which we can construct low-voltage translinear circuits and log-domain filters. A K-input MITE produces an output current that is exponential in a weighted sum of its K input voltages. We briefly discuss six MITE implementations and show experimental data from two of these six that we have fabricated in a 2-um double-poly CMOS process available through MOSIS.

WPA8-6 -- Very Low Charge Injection Switched-Current Memory Cell

Leelavattananon, Kritsapon, *Imperial College of Science, Technology and Medicine*

A new switched-current memory cell is proposed which achieves very low charge injection errors. The technique virtually eliminates the signal-dependent error, leaving only an offset which is cancalled using either dummy switches or a fully differential configuration. The improved memory cell was designed using a standard 3.3 V, 0.8 micron CMOS digital process. Simulation results demonstrate that the signal-dependent charge injection error is lowered by as much as two orders of magnitude.

WPA8-7 -- An Improved CMOS Offset-Compensated Current Comparator For High-Speed Applications.

Worapishet, Apisak, *Imperial College of Science, Technology and Medicine*

An improved CMOS current comparator suitable for use with either S2I or S3I switched-current cells is presented in this paper. The circuit also incorporates new design tehnique to enhance both speed and resolution. A practical CMOS design is presented and simulations show operation at 80MHz with 10 bit precision from a 3 V supply.

WPA8-8 -- Wideband Current-Mode Absolute Value Circuits

Lidgey, John, and Hayatleh, K., *Oxford Brookes University* and Porta, S. *Universidad Publica de Navarra*

Two wideband current-mode absolute value, or precision full-wave rectifier (PFWR), circuits have been designed and developed. They are transistor level based designs, ideally suited for ASIC realisation. The two different, architecture circuits are described. In the first design a comparator is used to control a current-steering circuit to achieve the required unipolar output response. The topology of the circuit exhibits high speed performance with minimum transients. The second design is a development from the first. The circuit has lower overall complexity and provides enhanced performance. It is based on an emitter-coupled common -collector, with a NPN Quasi-Darlington dynamic buffer. Both techniques show promising performance in terms of operating speed.

WPA9 – Amplifier Building Blocks
Chair: Jose Silva-Martinez
National Institute for Astrophysics, Optics, and Eng.

2:00pm – 5:30pm - ***Room: Bonzai III***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA9-2 -- A Current Driven, Programmable Gain Differential Pair Using MOS Translinear Circuits

Conti, Massimo, Crippa, Paolo, Guaitini, Giovanni , Orcioni, Simone, and Turchetti, Claudio, *University of Ancona*

In this paper a novel current-mode CMOS differential pair which uses the translinear principle is suggested. The shape of the sigmoidal input-output function can be adjusted through a tuning current over a wide operating range. A design example of the circuit applied to the implementation of an analog VLSI neural system is presented.

WPA9-3 -- New High-Precision Circuits For on-Chip Capacitor Ratio Testing and Sensor Readout

Wang, Bo, *Oregon State University*

This paper presents novel CMOS switched-capacitor circuits for high-accuracy on-chip capacitor ratio testing and sensor readout. Using sigma-delta and correlated-double-sampling (CDS) techniques, these circuits provide accurate digitized capacitive ratio readout. Simulation results show that the resolution can be as fine as 100 aF for 10 pF tested capacitors. One of the circuits was realized in fully integrated form. It provided readings with a standard deviation of less than 20 aF (2 ppm) for 10 pF capacitors.

WPA9-4 -- Voltage Clamping Current Mirrors with 13-Decades Gain Adjustment Range Suitable for Low Power MOS/Bipolar Current Mode Signal Processing Circuits

Linares-Barranco, Bernabe and Serrano-Gotarredona, Teresa, *National Microelectronics Center* and Andreou, Andreas G., *The Johns Hopkins University*

Low power current mode signal processing circuits require the two following conditions: (a) use of current mirrors to replicate and amplify/attenuate current signals, and (b) voltage clamping of those nodes with high parasitic capacitances so that the smallest current levels do not introduce unacceptable delays. In this paper we introduce two new active-input current mirrors that clamp their input node to a given voltage and which do not require compensation circuitry for stability. In conventional active-input current mirrors, input current cannot be made arbitrarily small, because this would produce oscillations. In the structures proposed in this paper current may spawn beyond six decades without requiring any compensation. Furthermore, the two new proposed current mirrors, if operated in weak inversion, can be made to have a continuously voltage controlled gain with a tuning range of up to 13 decades. The proposed active-input current mirrors can be operated either with MOS or bipolar transistors. Experimental results that attest these facts are provided.

WPA9-5 -- Matching Performance of Current Mirrors with Arbitrary Parameter Gradients Through the Active

Lan, Mao-Feng, Geiger, Randall, *Iowa State Univeristy*

Effects of threshold gradients at any angle across a die and through active devices on the matching characteristics of current mirrors are discussed. Results show a major improvement but also an unreported limitation in performance of common-centroid layouts. A CAD tool that predicts performance of arbitrary layouts under arbitrary parameter gradients is introduced.

WPA9-6 -- An Active Tuning and Impedance Matching Element

Lapinoja, Mikko J., and Rahkonen, Timo E., *University of Oulu*

An integrated circuit that operates as a voltage controlled admittance with a constant real part and variable imaginary part is presented. It consists of two differential pairs, the inputs of which are phase shifted with respect to each other and their transconductance ratio can be varied. The circuit can be used as a combination of an active varactor and amplifier in integrated LC type voltage controlled oscillators, or as a tunable impedance matching element in rf inputs or outputs to compensate adaptively for the impedance mismatch due to temperature drift or large signal effects, for example.

WPA9-7 -- Voltage Controlled Resistor for Mismatch Adjustment in Analog CMOS Circuits

Yu, Baiying, *Iowa State University*

A Voltage Controlled Resistor (VCR) scheme is demonstrated for use in precision analog applications on standard CMOS processes. This technique utilizes a metal or poly overlay across an n-well resistor field region to slightly modulate the well resistivity. This scheme is quite useful in data converters employing dynamic element matching and amplifiers employing offset cancellation as the maximum adjustable change in resistance is only slightly larger than typical component mismatches. This small voltage variability allows for simple but very precise calibration compared to traditional methods. A macro-model of the VCR is proposed based on device simulation results from ATLAS. Simulation of this device in a dynamic element matching circuit is also demonstrated.

WPA9-8 -- Harmonic Distortion in CMOS Current Mirrors

Bruun, Erik, *Technical University of Denmark*

One of the origins of harmonic distortion in CMOS current mirrors is the inevitable mismatch between the MOS transistors involved. In this paper we examine both single current mirrors and complementary class AB current mirrors and develop an analytical model for the mismatch induced harmonic distortion. This analytical model is verified through simulations and is used for a discussion of the impact of mismatch on harmonic distortion properties of CMOS current mirrors. It is found that distortion levels somewhat below 1% can be attained by carefully matching the mirror transistors but ultra low distortion is not achievable with CMOS current mirrors.

WPA10 –Oversampled and Sigma-Delta Techniques II
Chair: Phillip E. Pace
Naval Postgraduate School

2:00pm – 5:30pm - ***Room: San Carlos I***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA10-1 -- A Bandpass Sigma-Delta Demodulator

Keady, Aidan G., and Lyden, Colin, *National Microelectronics Research Centre*

A new architecture for bandpass Sigma-Delta A/D conversion/demodulation with particular application in radio reception is described. The proposed architecture is efficient in terms of silicon area usage and has improved performance over existing topologies. A chopping scheme shifts the signals from the passband to DC and a lowpass modulator is then used to perform the conversion. In the new implementation, the passband location is limited only by the maximum sampling rate achievable rather than the lower maximum modulator clock rate. Hence, the new converter can digitize bands at much higher frequencies than previous implementations, while an intrinsic anti-aliasing filter means that external anti-aliasing filter requirements are relaxed compared with undersampling converters. Simulation results are presented showing the operation of the converter with a QPSK-modulated input.

WPA10-2 -- A 5 GHZ continuous time Sigma-Delta modulator implemented in 0.4um InGaP/InGaAs HEMT technology

Olmos, Alfredo, *Laboratorio de Sistemas Integraveis Univ. Sao Paulo*

The design of a second-order continuous-time Sigma-Delta (SD) modulator working at a sampling rate of 5GHz and implemented on a 0.4um InGaP/InGaAs HEMT technology is described. A new polarity alternating feedback (PAF) technique is presented and applied to the design of a high sampling frequency comparator. The fully differential architecture adopted for the modulator includes the PAF comparator and pairs of highly linear V-I converters, high-speed opamps, and high-speed 1-bit DAC units. At a sampling rate of 4.9GHz and a signal bandwidth of 100MHz, the circuit achieves 43dB signal-to-noise ratio (SNR), which is equivalent to 7.2 bits resolution. The modulator occupies a total area of 0.9mm2 dissipating 400mW from a 3.2V power supply. The exceptional performance we attained corresponds to the highest sampling rate and lowest power consumption for an oversampled AD converter in III-V technology known to us.

WPA10-3 -- A 50 MHz Continuous-Time Switched-Current Sigma-Delta Modulator

Luh, Louis, Choma, John, and Draper, Jeffrey, *University of Southern California*

A new architecture of second-order continuous-time switched-current Sigma-Delta motedlator is presented. A Reference Current Generator is used in the second stage to solve the scaling problem. A novel current switch is designed to minimize the clock feedthrough problem and increase the operating speed. With a 50 MHz sampling rate, it has achieved 50 dB dynamic range (8-bit) at 1 MHz. This modulator has been fabricated in a 2um CMOS process with an active area of 0.37 mm^2. The power dissipation is 15 mW.

WPA10-4 -- A Multi-Bit Sigma-Delta Modulator with Interstage Feedback

Fang, L., and Chao, K.S., *Texas Tech University*

A multi-bit sigma-delta modulator with interstage feedback is described. The structure employs a single-bit quantizer in the main sigma-delta modulator and a multi-bit quantizer in the feedforward path with its error fed back to the main modulator. It combines the advantages of sigma-delta modulator and pipeline A/D converters. This system topology offers an additional noise shaping factor to the error of the multi-bit quantizer.

WPA10-5 -- Approaches to Simulating Continuous-Time Delta Sigma Modulators

Cherry, James A., Snelgrove, W. Martin, *Carleton University*

Several different approaches for the simulation of continuous-time delta sigma modulators are listed, and their tradeoffs in terms of realism vs. simulation speed are examined. Apart from the moderately-obvious methods of directly implementing the system differential equations (fast) and full circuit-level simulation using SPICE (slow), a new method based upon the equivalence between continuous- and discrete-time filters inside the delta sigma loop is reported herein, with illustrations of its application.

WPA10-6 -- Architectural Coefficient Synthesis for the Implementation of Optimal Higher-Order Delta-Sigma Analog-to-Digital Converters

Fiez, Terri, and Naiknaware, Ravindranath, *Washington State University*

This paper describes a method to synthesize architectural coefficients for higher-order delta-sigma modulators. Considerations for maximum dynamic range and optimal power are addressed. First, a modulator with optimal theoretical performance is synthesized. Then, the theoretical delta-sigma ADC is scaled to make it realizable with maximum dynamic range, and finally, the modulator is further modified for optimal power and area performance. During each of the steps, the modulator theoretical performance and stability characteristics are preserved. Construction of an optimal seventh-order modulator is demonstrated. It is also shown that the coefficient synthesis significantly affects the power and area consumption.

WPA10-7 – Loop Delay and Jitter in Continuous-Time Delta Sigma Modulators

Cherry, James A., and Snelgrove, W. Martin, *Carleton University*

The effect of certain fundamental nonidealities on the resolution of a continuous-time (CT) delta sigma modulator are examined in this paper. We start by talking about the equivalence between an ideal CT delta sigma modulator and its discrete-time (DT) counterpart, then consider the effect of quantizer/DAC propagation delay, clock jitter, and the recently-identified phenomenon of signal-dependent jitter on the ideal performance.

WPA10-8 -- Digital Correction of Non-Ideal Amplifier Effects in the MASH Modulator

Davis, Alan J., and Fischer, Godi, *University of Rhode Island*

An approach to remove the effects of amplifier finite gain and C-ratio mismatches in the MASH sigma-delta modulator is presented. By adding a digital correction term to the output of the digital noise cancellation filter, the parasitic quantization noise terms can be removed for all but the final stage, eliminating the intermediate quantization noise terms due to non-ideal integrators. Using this technique, the MASH can approach the performance of an ideal third-order modulator. We have confirmed an SNR+THD of 105.6 dB via a behavioral simulation of the MASH using an amplifier open-loop gain of only 500 and capacitor matching errors as large as of 1.0 %.

WPA11 – Device Modeling
Chair: Kartikeya Mayaram
Washington State University

2:00pm – 5:30pm - ***Room: San Carlos II***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA11-1 -- Modeling, Extraction and Simulation of CMOS I/O Circuits under ESD Stress

Li, Tong, *Univ. of Illinois at Urbana-Champaign*

A CAD tool set for VLSI CMOS I/O circuit design is developed. It includes a circuit simulator, a layout extractor and a substrate resistance solver. This paper presents a new layout extractor for CMOS I/O circuits and a new method for modeling the substrate resistance. With these tools, for the first time, full I/O circuits can be simulated accurately at the circuit-level with consideration of the substrate-coupling effects. The CAD tools are demonstratively applied to an industrial circuit.

WPA11-2 -- Single-Event Effects in Micromachined PMOSFETs

Osman, Ashraf A.; Mojarradi, Mohammad and Mayaram, Kartikeya, *Washington State University*

Single-event effects in micromachined PMOSFETs in a 2um standard CMOS process are examined using device simulation. A comparison with the bulk and SOI PMOSFETs with comparable structures is also provided. The effects of N-well depth, angle of incidence, and N-well contact have been investigated in micromachined transistors. The substrate current and collected charge in micromachined PMOSFETs with thin N-wells are significantly lower compared to bulk PMOS devices.

WPA11-3 -- A Generalized HSPICE Macro-Model for Pseudo-Spin-Valve GMR Memory Bits

Black, William C. and Das, Bodhisattva, *Iowa State University*

Nonvolatile semiconductor storage using Giant-Magneto-Resistance (GMR) memory bits has the potential for revolutionizing both high density and high speed memory applications with devices exhibiting unlimited write endurance and very low required write energy. This work presents the first generalized circuit macro-model for a pseudo-spin-valve GMR memory bit. The macro-model is realized as a four terminal sub-circuit which emulates GMR bit behavior over a wide range of sense and word line currents. The non-volatile and nonlinear nature of GMR memory bits are accurately represented by this model and simulations of non-volatile GMR latch structures with HSPICE show expected outcomes. The model is flexible and relatively simple: ranges of the write /read currents and bit resistance values are incorporated as parameterized variables and no semiconductor devices are used within the model.

WPA11-4 -- Compact SPICE Modeling and Design Optimization of Low Leakage a-Si:H TFTs for Large-Area Imaging Systems

Arokia, Nathan, *University of Waterloo*

We present a SPICE model that takes into account the different mechanisms underlying the reverse leakage current in hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs). The main source of leakage current in these devices appear to arise from the parasitic reverse-biased p-i-n diode at vicinity of the drain. At low gate voltages, the diode's reverse current can be attributed to thermal generation of electrons from the valence to conduction bands through mid-gap states in the a-Si:H. At high gate voltages, the reverse current is due to trap-assisted tunneling, whereby electrons tunnel to the conduction band through mid-gap states. This bias dependent behavior has been modeled and implemented in SPICE using simple circuit elements based on voltage controlled current sources. Simulated and measured leakage current characteristics are in reasonable agreement.

WPA11-5 -- SPICE model for Mechanically Stressed Device/Circuit Simulation

Maier, Christoph; Steiner, Ralph; Mayer, Michael; Vogt, Rolf, and Baltes, Henry, *ETH Zuerich*

We present a SPICE-compatible circuit model to predict the effects of mechanical stress on the electrical characteristics of devices and integrated circuits (ICs). The model is assembled from unit cells, which consist of resistors and voltage controlled current sources. We verified the circuit model with measurements on an n-well magnetic sensor structure on (100) silicon. The model predicts the influence of stress to less than 10% discrepancy from measurement.

WPA11-6 -- Rapid Extraction of Capacitance in a-Si Imaging Arrays

Nathan, Arokia and Pham, Hoan H., *University of Waterloo*

We present a new technique for computation of charge density for a multi-conductor system embedded in homogeneous or multiple dielectric media. The charge density distribution determines the parasitic coupling capacitance in large-area imaging arrays or ULSI interconnects, as well as the electrostatic interaction in MEMS. The proposed scheme employs the exponential-expansion-based method for efficient evaluation of the three-dimensional potential and electric field. Here, the memory requirement is independent of the desired degree of accuracy, which is an important feature for large-scale simulation involving panel numbers in the range of a few hundred thousand or several million.

WPA11-7 -- An Efficient MOS Transistor Charge/Capacitance Model with Continuous Expressions for VLSI

Sheu, Bing J., *University of Southern California,*

A unified modeling approach for the submicron MOS transistor charge/capacitance characteristics in all operation regions is presented. The development of MOS charge model is based on the charge density approximation to reduce the complexity of the expression. The unified charge densities in gate, channel, and bulk are obtained with assistance of the sigmoid, hyperbola, and exponential interpolation techniques. By carrying out the integration of the charge densities along the channel area, the terminal charges associated with gate and bulk can be obtained. The non-reciprocal capacitance behavior is well realized in this model. Good agreement between the measurement data and simulation results is obtained.

WPA11-8 -- Wavelet-Based Galerkin Method For Semiconductor Devices Simulation

Chan, Chung-Kei Thomas and Chang, Fung-Yuel, *The Chinese University of Hong Kong*

Using wavelet methods, local high order schemes can be constructed near the singularities. Moreover, the stiffness matrix is sparse and can readily be inverted due to the compact support property of wavelets. An adaptive Galerkin-wavelet method for semiconductor devices simulation is presented. A set of wavelet bases can be chosen adaptively for each iteration according to the error levels. So, computational time is saved and hence a more accurate result can be obtained by including higher order terms. Also, an elegant way to handle the boundary conditions is provided. A simulation of an abrupt P-N junction is used to demonstrate this effectiveness in this paper.

WPA12 – Filters and Electornics Circuits
Chair: Ray Chen
San Jose State University

2:00pm – 5:30pm - ***Room: San Carlos III***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA12-1 -- Stability of a Continuous-Time State Variable Filter with ORA-L and Current Amplifier Integrators

Bakken, Tim W. and Choma, Jr., John, *University of Southern California*

The stability of a continuous-time state variable filter is analyzed using the Routh-Hurwitz criterion. This criterion assesses stability by indicating the number of poles that lie in the right-half plane. The filter is examined separately with integrators implemented with an ORA-L and a current amplifier. Both amplifier types are characterized by a dominant-pole frequency response, and the stability of each implementation is compared. HSPICE simulations confirm the theoretical analyses, which indicate that the bandwidth of the ORAs and current amplifiers must be much larger than the desired frequency of operation to ensure stability. Since the analyses assume a dominant-pole response, all higher-order poles of the actual amplifier must also be much greater than the unity-gain frequency to minimize excess phase.

WPA12-2 -- A New Direct Digital Frequency Synthesizer Architecture for Mobile Transceivers

Hegazi, Emad Mahmoud; Ragaie, Hani Fikry; Haddara, H.; and Ghali, H., *In Shams University*

A new architecture for Direct Digital Frequency Synthesizer (DDFS) with constant Oversampling ratio (OSR) is proposed. The architecture contains no ROM block. The switching pool of the Digital to Analog Converter (DAC) is simplified allowing a 90% reduction in DAC settling time. The basic concepts of the proposed architecture are discussed and simulation results are demonstrated.

WPA12-3 -- A Second-Order Log-Domain Bandpass Filter for Audio Frequency Applications

Edwards, Robert Timothy and Cauwenberghs, Bert, *Johns Hopkins University*

Log-domain filters have recently come into the limelight of the VLSI community as an important class of circuits for implementing continuous-time filters in the current domain. Some papers have discussed log-domain circuit analysis and some have addressed circuit synthesis. In this paper we describe synthesis of a second-order log-domain bandpass filter, address issues related to low-frequency (audio-frequency) filter design, and show experimental results from systems fabricated in standard 2um and 1.2um BiCMOS technologies.

WPA12-4 -- A Theory of Information Network Analyzer PPN

Shinomiya, Norihiko and Wantanabe, Hitoshi, *Soka University*

This paper proposed an information network analyzer PPN (Parallel Processing Network) which is composed of the same processing capabilities as that of the object network, and presented properties of a PPN with Node-Potential or the minimum number of edges from the base-node. Algorithms of system change (extension or reduction) of an information network are presented. As an application of node-potential, a rooted-tree finding algorithm is introduced, that gives a protocol for the multicast routing in an information network. Utilizing the solutions of these fundamental and experimental results, it is shown that PPN can provide useful means for various network analyses.

WPA12-5 -- CMOS Precision Half-Wave Rectifying Transconductor

Jun, Sibum, LG *Semicon Co., Ltd.* and Ahn, Su Jin, *POSTECH*

A novel CMOS half-wave rectifying transconductor is presented. The proposed circuit utilizes a simple new cascode current subtracter which is obtained from conventional cascode current mirror by a judicious reconfiguration to yield additional subtrahend signal path. The simulated DC transfer characteristics is highly linear up to 1.5V differential input voltage and the blunt corner at zero-crossing is 20mV. The total harmonic distortions at 100kHz with 1.5Vp-p in the positive half cycle are better than -46.5dB. The usable operating frequencies are up to 10MHz with maximum peak-to-peak input voltage and 75uW power consumption.

WPA12-6 -- Analysis of Limit-Cycle Oscillations in a Log-Domain Filter

Fox, Robert M., *University of Florida*, and Ferrer, Enrique, *Motorola Inc.*

A circuit is presented for a class-AB fully differential log-domain parallel resonator. If floating rather than shunt capacitive loads are used, the circuit can be triggered into steady-state limit-cycle oscillations by large-enough transient input stimuli. The nature of the instability is explored. Transient analysis in SPICE is used to locate the separatrix between stable-equilibrium-point-seeking and limit-cycle-seeking regions of state space.

WPA12-7 -- Large Signal Models for Oscillator Design

Kukk, Vello, *Tallinn Technical University*

Large signal models needed for fast time domain modelling of oscillator circuits are considered. The models are based on harmonic linearization and derived for conventional time domain simulators. The paper describes the techniques for the use of first harmonic of driving signal only. The model consists of three coupled parts: DC, real, and imaginary subcircuits. Building of those subcircuits for exponential non-linearity is simple and could be recommended as basic for other nonlinearities. Several modelling experiments with oscillator circuits are shortly reviewed.

WPA12-8 -- An Approximate Analytical Approach for Predicting Period-Doubling in the Colpitts Oscillator

Maggio, Gian Mario and Kennedy, Michael Peter, *University College Dublin*, and Gilli, Marco, *Politecnico di Torino*

In this paper we present a ne method for approximating the period-doubling locus of a piecewise-linear model of the Colpitts oscillator. This method exploits harmonic balance techniques for solving the variational equation associated with a generic limit cycle. In this way conditions for a period-doubling bifurcation are derived.

WPA13 – Multimedia/Communications **Poster Session**
Chair: Tsuhan Chen
Carnegie Mellon University

2:00pm – 5:30pm - ***Room: Serra Ballrom - Back I***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA13-1 -- Low Complexity Equalization for Cable Modems

Wolf, Tod D. *Texas Instruments Inc.*

Cable modems are a relatively recent development in the internet access business in which the residential user has a high speed link to his home over the coaxial cable plant. In previous cable modem designs the equalizer, an adaptive filter that compensates for distortion in the coaxial cable, dominates the chip area, at about 50%. A significant reduction in equalizer size will therefore reduce the cost and complexity of the overall chip significantly. In this paper we describe a design that takes advantage of the relatively low sample rate of the cable modem equalizer to reduce the complexity of the equalizer. We show that a length 12 complex equalizer with full LMS update can be implemented with only four

multipliers using an 80MHz clock. For the decision feedback equalizer we implement a minimum gate width 12 by 4 multiplier using 0.35 um technology. This design demonstrates a way of reducing circuit complexity.

WPA13-2 -- A Consideration on the Computatonal Requirements of Blind Equalization Using the Orthogonal Projection

Kitaoka, Yoshihiro, *Fukuoka Institute of Technology;* Matsumoto, Hiroki, *Maebashi City College of Technology* and Furukawa, Toshihiro, *Fukuoka Institute of Technology*

The equalization using the traditional blind estimation is based on the channel outputs and knowledge of the probabilistic property of input signal. But it is difficult for conventional to be implemented with on-line processing because the traditional algorithms need high-order momentum. We present a new method using the orthogonal projection, in order to enable the on-line processing of blind equalization. First, we will estimate the characteristics of the channel using both the skewness and the kurtosis of the output of the channel. Secondly, we will design an equalizer using the orthogonal projection onto the received signal space. The proposed method is based on designing an equalizer parameter so that the matrix PN,N = WN,N HN,N may be the orthogonal projection matrix onto the received signal space, where WN,N and HN,N demote the impulse response matrix of an equalizer to be designed and that of the channel respectively. The impulse response matrix of an equalizer is basically expressed with Moore-Penrose inverse matrix. The proposal blind equalization algorithm can be implemented on-line processing, it is expected that the convergence characteristics of the proposed is better than that of the traditional.

WPA13-4 -- A Novel MPEG Audio Degrouping Algorithm

Tsai, Tsung-Han, Chen, Liang-Gee, Chang, Hao-Chieh, and Huang, Sheng-Chieh *National Taiwan University*

Degrouping is the key component in MPEG Layer II audio decoding. It mainly contains the arithmetic operations of division and modulo, which requires lots of hardware and computation time. In this paper, we propose a novel degrouping algorithm with a low complexity design concept. By using mode selection and iterative decomposition, only the addition and subtraction are needed. The elimination of the multiplier, divider and ROM table can therefore extremely saves a lot of chip area, but still keeps the high efficiency without loss of any accuracy.

WPA13-5 -- A Robust Algorithm for Formant Frequency Extraction of Noisy Speech

Zhao, Qifang, *Saitama University*

In this paper a new method for formant frequency estimation of noisy speech is proposed based on the linear prediction analysis. Usually the linear prediction analysis based algorithms can extract the formant frequencies effectively for clean speech. When speech is corrupted by noise, however, their performances degrade seriously. It is well known that the autocorrelation function has the property of concentrating the energy of the white noise on the nearby of the zero lag. Utilizing this property of the autocorrelation function, the proposed method extracts the formant frequencies from the autocorrelation function of the speech instead of the speech itself. The experimental results show that the proposed method is much more robust to noise than the conventional linear prediction based algorithms.

WPA13-6 -- Realization of Multiwavelet-Based Transform Kernels for Image Coding

Rieder, Peter, Schimpfle, Christian V.and Nossek, Josef A., *Munich University of Technology*

In this paper the efficient implementation of discrete multi-wavelet transforms is examined. These transforms can be used for image coding. The presented architecture is based on lattice structures and computationally efficient CORDIC-based m-rotations. An exemplary VLSI-implementation for a multiwavelet-based lapped orthogonal transform is presented.

WPA13-7 -- Asynchronous VLSI Architectures for Huffman Codecs

Hauck, Oliver Friedrich, *Darmstadt University of Technology;* Sauerwein, Helmut, *BetaResearch;*and Huss, Sorin Alexander
Darmstadt University of Technology

A novel asynchronous VLSI architecture for Huffman codecs employing fixed code books is presented. The main idea is to layout the Huffman tree in hardware and to exploit signal statistics via asynchronous logic thus avoiding expensive pipelining. This approach applies to encoders and decoders as well. The resulting circuits are both compact and fast. Post-layout HSpice simulations of an encoder tree demonstrate their efficiency. A comparison of two-phase and four-phase protocol results in only a marginal speed advantage of two-phase while incurring significant overhead and a more difficult design.

WPA13-8 -- A Perceptual Based Rate Control Scheme for MPEG-2

Chan, Shing Chow, *The University of Hong Kong*

In this paper, a new perceptual based rate control algorithm for MPEG-2 is presented. The algorithm first determines the target bit count for each frame using simple statistical models. Precise bit allocation is used to adjust the macroblock quantization scale factors to meet the given bit count, with the uniform visual fidelity as the primary objective. Since the buffer is very stable, it is less sensitive to transmission delay. Experimental results showed that it gave better visual quality and less buffer variations as compared to the TM5 rate control scheme.

WPA13-9 -- Fast Time Scale Modification using Envelope-Matching (EM-TSM)

Au, Oscar C., and Wong, W.C., *The Hong Kong University of Science and Technology*

Time scaling of speech and audio signals is one of the key features of the upcoming MPEG4 standard. Synchronized Overlap-and-Add (SOLA) is a time scaling algorithm known to achieve good speech quality. One problem of SOLA is that it requires a large amount of computation in the search of the best matching point between the analysis and synthesis frames. This is especially serious when multiple time scaling factors are to be supported as in the case of MPEG4. In this paper, we propose a technique called envelop-matching to simplify the computation with effectively the same quality. In envelop-matching, zero crossing locations are used as features for the search. We propose a very fast algorithm for the distortion computation.

WPA13-10 -- Performance Study of Time Delay Estimation in a Room Environment

Jian, Ming, *Nanyang Technological University*

Time delay estimation (TDE) is often used for source localization in microphone arrays and the performance of TDE is always affected by the reverberation in a room. In this paper, the performance of TDE in a rectangular room environment is studied for microphone arrays. The probability of anomalies of time delay estimates is obtained theoretically for the multi-path propagation in the room. The effects of the room reverberation on the TDE under different microphone patterns, microphone position configurations and spacings between the microphones are evaluated.

WPA14 – Neural Networks **Chair: Mona Zaghloul** *George Washington University*	**Poster Session**
2:00pm – 5:30pm -	***Room: Serra Ballroom – Back II***
*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*	

WPA14-1 -- Low Complexity CMOS Competitive Array for Approaching Asssignments

Gomez-Castaneda, Felipe; Flores-Nava, Luis M.; and Moreno-Cadenas, Jose A., *Center for Research and Advanced Studies of the NPL*

This work presents a CMOS analog integrated circuit in which an array of 8x8 winner-take-all neural units or competitive units computes binary matrices as an approach to the solution of assignment problems. The small silicon area in this system results from using early low-complexity current-mode circuits. The dynamic performance for selecting winning units by this prototype analog integrated circuit that encodes permutation matrices is evaluated with PSpice simulations.

WPA14-2 -- An Artificial Model for Biological Computation and Control for a Locomotion System

Curran, K. and Wooten, E., *U. S. Naval Academy*; and Newcomb, Robert W., *University of Maryland*

Each discipline has its own methods of modeling its components and developing the mathematical analysis of the systems which they want to describe. Investigating these systems from different perspectives can provide a means of discovering system operation. Specifically, when approaching the reverse engineering of a biological system, the best description of the elements should include the biological parameters and their known relationships. The modeling should be carefully tied to the biological experimental data and the results of the simulations should provide outputs comparable with actual output data from the original system. Once the model has been thoroughly tested, the mathematical description of the model can be redefined with new variables of interest for the discipline involved. This paper describes the design of a neural network capable of providing simulated output comparable to the deafferented flight neural control behavior of the locust, using GENESIS (General Neural Simulation System).

-- An Efficient Method of Automatical Feature Extraction and Target Classification

Zhang, Yanning and Jiao, Licheng, *Xidian University*

P.R. China's fishery and offshore petroleum development have been in urgent need of a classifier of noise signals. In this paper, The feature extraction mechanism and the classification mechanism of the adaptive wavelet neural network are revealed by mathematical analysis and an efficient engineering classifier based on the adaptive wavelet neural network is designed and applied to classify the actual ship noises. The classification experiment results show that the mathematical analysis of the feature extraction mechanism and the classification mechanism is correct and provides theoretical bases for the adaptive wavelet neural network classifier design

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WPA14-4 -- Pseudorandom Generator based on Clipped Hopfield Neural Network

Zhang, Yanning and Jiao, Licheng, *Xidian University*

We present a new construction of a pseudorandom generator based on a single linear feedback shift register and a clipped version of Hopfield neural network. The clipped Hopfield neural network (CHNN) acts as a nonlinear filter function, which destroys the linearity and algebraic structure of the LFSR. The resulting sequences have long period and large linear complexity. The construction is suitable for practical implementation of efficient stream cipher cryptosystems.

WPA14-5 -- Global Stability of a Larger Class of Dynamical Neural Networks

Arik, Sabri, *Istanbul U niversity*

In this paper, we present a sufficient condition for the existence, uniqueness and global asymptotic stability (GAS) of the equilibrium point for a larger class of dynamical neural networks. It is shown that the digonal dominance of the interconnection matrix guarantees the existence, uniqueness and GAS of the equilibrium point with respect to all nondecreasing activation functions.

WPA14-6 -- Hardware Realization of a Hamming Neural Network with On-Chip Learning

Schmid, Alexandre; Leblebici, Yusuf; and Mlynek, Daniel, *Swiss Federal Institute of Technology Lausanne*

This paper addresses the mixed analog-digital hardware implementation of a Hamming artificial neural network with on-chip learning. The developed integrated circuit architecture consists of a charge-based variable-weight neural network, and a digital module implementing the chip control, as well as the on-chip learning algorithm as a hardware-oriented adaptation of the well-known error-correction algorithm. Both the analog and the digital parts interact with each other to perform a pattern recognition task. A dedicated digital memory unit acts as the interface to temporarily hold the newly processed weights. We describe the actual realization as well as the design-flow which led to this development, including C software simulation, full-custom design and automated VHDL-based synthesis.

WPA14-7 -- Car Plate Recognition by Neural Networks and Image Processing

Parisi, Raffaele; Lucarelli, G.; and Orlandi, G., *University of Rome "La Sapienza"*

In this paper we describe an experimental system for the recognition of Italian-style car license plates. Images are usually taken from a camera at a toll gate and preprocessed by a fast and robust 1-D DFT scheme to find the plate and character positions. Characters are classified by a multilayer neural network trained by the recently developed BRLS learning algorithm. The same neural network replaces both the traditional feature extractor and the classifier. The percentage of correctly recognized characters reaches the best scores obtained in literature, being highly insensitive to the environment variability, while the architecture appears best suited for parallel implementation on programmable DSP processors.

WPA14-8 -- Architecture and Design Methodology of the RBF-DDA Neural Network

Aberbour, Mourad and Mehvez, Habib, *University de Pierre et Marie Lovie*

This paper presents a novel implementation of the RBF-DDA (Radial Basis Functions - Dynamic Decay Adjustment) neural network. We will investigate the architectural design and the hardware implementation. The features of this design are the possibility of mapping the architecture on different standard cells libraries as well as FPGA's, and mainly its modularization. This is an example which reflects the new trend in design methodologies relying on re-use and IP blocks. Indeed, the architecture is implemented using intensively the module generator and macro-blocks concept. The design is thus readily reusable, flexible and upgradable. The architecture is parameterized in terms of the precision of the data processed by the network and in terms of the size of the network itself (number of neurons). The neural network is used in the classification of the image signatures which are extracted from gray-level images using the Gabor-Morlet wavelets and some data compression schemes.

WPA14-9 -- Hardware Implementation of Post-Retinal Processing using Analog VLSI

Satakopan, S.; James, S.; and Akers, Lex, *Arizona State University*

Study of nature has always given us the path to do things in a smart and efficient way. In the field of image processing we feel that the retinal vision system might provide us with some insight. The visual cortex of the mammalian brain allows compact image coding and representation. On the basis of measured receptive field profiles and spatial frequency tuning characteristics of simple cortical cells, it can be concluded that the representation of an image in the visual cortex must involve both spatial and spatial frequency variables. These localized spatial and spatial frequency filters found in the visual cortex of the mammalian brain resemble Gabor filters. We have developed a chip with photoreceptors interfaced to these filters.

WPA14-10 -- High Performance Programmable Bi-Phasic Pulse Generator Design for a Cochlear Speech Processor

Ay Suat; Sheu, Bing; and Zeng, Fan-Gang, *University of Southern California*

Cochlear implant devices are designed to provide sound sensation and improved speech understanding to people who are profoundly hearing impaired. Best speech recognition could be achieved by using multi-channel, multi-electrode cochlear implant devices. In a multichannel cochlear prosthesis, channel interaction and tissue damage are important issues to be solved. Speech processing and modulation strategies are the steps in solving these problems. Bi-phasic pulse streams are used as a modulator signal in Continuous Interleaved Sampling (CIS) base cochlear implant devices which is the best processing strategy. In this paper, we present a high-performance, low-power, low-voltage, digitally programmable bi-phasic pulse generator for cochlear implant speech processing systems operates at a single 1.5 V, and consumes only 15 uWatt dynamic power. Pulse width and inter-channel separation time periods of 4 channels can be digitally programed with 15 programing choices.

WPA14-11 -- Pulse Stream based CNN Hardware Implementation

Colodro, Francisco; Torralba, A.; Carvajal, R.G.; and Franguelo, L.G., *Escuela Superior de Ingenieros*

This paper presents the application of Pulse Stream Techniques (PSTs) to the hardware implementation of a Cellular Neural Network. The time differential equations of this networks suggest that the dynamic of one neuron status can be emulated by adding discretized packets of charge to a capacitor. This task can be carried out by driving a current source with a pulse stream signal. The stochastic representation of internal signals reduces hardware complexity.

WPA14-12 -- Design of Cellular Neural Networks with Space-Invariant Cloning Template

Lu, Zanjun and Liu, Derong, *Stevens Institute of Technology*

This paper presents a new synthesis procedure (design algorithm) for cellular neural networks with space-invariant cloning template with applications to associative memories. In the present synthesis procedure, the design problem is formulated as a set of linear inequalities and the inequalities are solved using the well-known perceptron training algorithm. When desired memory patterns are given by a set of bipolar vectors, it is guaranteed that a cellular neural network with space-invariant cloning template can be designed using the design algorithm developed herein. A specific example is included to demonstrate the applicability of the methodology developed herein.

WPA14-13 -- On the Stability of CNNs with Continuous Time Delay

Lei Xu, Xiaofeng Liao, *Department of Computer Science and Enginerring, The Chinese University of Hong Kong*

The stability of cellular neural networks with continuous time delay is investigated in the present paper. A main theorem related to the existence and boundedness of the solution for this kind of CNN's, as well as its global asymptotical stability is derived. Some numerical simulation examples aimed at justifying the theoretical results are also given.

WPA14-14 -- Synthesis of a Recurrent Double-Layer Transistor Network for Early-Vision Tasks

Barbaro, Massimo; Nazzaro, Antonio; and Raffo, Luigi, *University of Cagliari*

In this paper we present a double-layer transistor network, useful for early-vision embedded systems, able to convolve a sensorial input with a Gabor kernel. The network, whose main advantages are low power consumption, compactness of physical implementation and full programmability of the convolution kernel, has been simulated and successfully compared with theoretical expectations.

WPA14-15 -- Harmonic Retrieval Using Higher-Order Statistics and Hilbert Transform

Li, Shenghong and Liu, Zemin, *Beijing University of Posts and Telecommunications*

So far, the problem of harmonic retrieval with quadratic phase coupling in colored non-Gaussian noise has not been solved well. For this reason, this paper presents a new approach for harmonic retrieval in colored non-Gaussian ARMA noise, and further, another new approach is given for harmonic retrieval in mixed Gaussian and colored non-Gaussian ARMA noises. Both of the approaches can realize harmonic retrieval whether the harmonic signal contains the components of quadratic phase coupling or not. Simulation results show the effectiveness of the two approaches.

WPA14-16 -- Segmentation Coding for Object-Based Attentive Selection Systems

Wilson, Charles S., *Georgia Institute of Technology*; Morris, Tonia G., *Intel Corporation*; and DeWeerth, Stephen P., *Georgia Institute of Technology*

In this paper we present an analysis of a segmentation coding algorithm used in object-based visual attentive selection systems. This coding algorithm segments images into objects, and assigns a segmentation code to each object. The objects then compete for attention in the selection process. Thus, these systems use a biologically-inspired technique to balance the need for high-speed processing and the abundance of input image data. We have implemented these systems in 2.0m and 1.2m CMOS processes.

WPA14-17 -- Current-Mode Truth Value Evaluation Circuits for Complementary Fuzzy Logic Systems

Chen, Chien-Yau; Yu, Gwo-Jeng; and Liu, Bin-Da, *National Cheng Kung University*

In this paper, a set of simple-structure current-mode truth value evaluator circuits for sentential operations, called negation, conjuction, disjunction, implication, and equivalence, in complementary fuzzy logic systems are proposed. They perform the desired function well at high speed with 140ns/450ns rise time/fall time and error less than 0.5% of full-scaled current (15ua). On the average, the power consumption of these circuits is about 255uW at 5V power supply voltage.

WPA14-18 -- A Hybrid Fuzzy Neural Decoder for Convolutional Codes

Wu, Meng;, *Nanjing University of Posts and Telecommunications*; Zhu, Wei-Ping, *Concordia University* and Nakamura, Shogo, *Tokyo Donki University*

In this paper we propose a hybrid fuzzy neural network for decoding of convolutional codes. The decoding process will be completed by classifing of the proposed network instead of conventional decoding methods such as Viterbi algorithm. According to the encoding principle of convolutional codes, the size of the network is determined dynamically through clustering. Logic operations are also used in the network, so the training speed of the network is very fast: only one or several iterations are required. Moreover we define fuzzy membership function for each hidden node, which enhances the associative capability of the network, thus improves the rectifing capability of the network. For the small constrain length we study the performance of the propose method and compare the Viterbi algorithm in detail.

WPA14-19 -- A New Edge-Preserving Smoothing Filter Based on Fuzzy Control Laws and Local Features

Muneyasu, Mitusji; Wada, Yuji; and Hinamoto, Takao, *Hiroshima University*

This paper proposes a new type of edge-preserving smoothing filter to be applied to an image corrupted by impulsive and white Gaussian noise. This filter is based on a weighted mean filter having two kinds of coefficient for impulsive and white Gaussian noise. These coefficients can be varied adaptively by local features in the window. Fuzzy control laws that can be used for the implementation of the proposed filter are described. To reduce the computational burden, the fuzzy inference model proposed by Ichihashi et al. is employed.Finally, the effectiveness of the proposed technique is shown by using results from a simulation.

WPA14-20 -- Current-Mode Circuit to Realize Fuzzy Classifier with Maximum Memebership Value Decision

Chen, Chuen-Yau; Tsao, Ju-Ying; and Liu, Bin-Da, *National Cheng Kung University*

A current-mode circuit to realize a fuzzy classifier is proposed in this paper. It is composed of two principle building blocks including the Euclidean distance calculator and the membership degree calculator. This classifier circuit is designed in modular methodology for easy expansion. To consider the proposed circuit more practically, the nonideal effects, such as body effect, channel length modulation, and device matching problem are also discussed. This classifier has been simulated with HSPICE in level 28 model and fabricated with 0.6 um single-polysilicon-double-metal CMOS process. The experimental results are in agreement with the simulated results. The hardware realization allows this classifier to operate in parallel rather than in serial as software-level verification does.

WPA14-21 -- A Novel CMOS Analogue Fuzzy Inference Processor

Song, C.T. Peter; Q uigley, Steven Francis; and Pammu, Sridhar, *University of Birmingham*

In this paper, we present a design of an analogue fuzzy inference processor with emphasis on the simplicity of architecture, circuitry and implementation. A brief overview of fuzzy inference processor building blocks suitable for hardware implementation using analogue Complementary Metal Oxide Semiconductor (CMOS) techniques will be presented. Techniques for generalising the design into an n-rule, n-input fuzzy processor have been established. The design of an analogue fuzzy processor with 4-rule aggregation is discussed, based on a standard 2 micron N-well process.

WPA14-22 -- Mixed-Mode VLSI Implementation of Fuzzy ART

Cohen, Marc H.; Abshire, Pamela; and Cauwenberghs, Gert, *Johns Hopkins University*

We present an asynchronous mixed analog-digital VLSI architecture which implements the Fuzzy Adaptive Resonance Theory (Fuzzy ART) algorithm. Both classification and learning are performed on-chip in real-time. Unique features of our implementation include: an embedded refresh mechanism to overcome memory drift due to charge leakage from volatile capacitive storage; and a recoding mechanism to eliminate and reassign inactive categories. A small scale 1.2um feature size CMOS prototype with 4 inputs and 8 output categories has been designed and fabricated. The unit cell which performs the fuzzy min and learning operations measures 100um by 45um. Experimental results are included to illustrate performance of the unit cell.

WPA14-23 -- A Cellular Nonlinear Network for Digital Error Correction

Kananen, Asko Tapio; Paasio, Ari Juhani; Lindfors, Saska; and Halonen, Kari, *Helsinki University of Technology*

A new concept for correcting errors in digital code is presented. For this purpose a programmable cellular nonlinear network can be used. To achieve high operation speed the high gain output nonlinearity is used. Positive range nonlinearity is combined to the high gain in order to achieve robust operation. The programmability of the network is reduced to only those coefficients actually needed in the processing to further increase the processing speed. An example of this coding scheme is given where the ``bubbles'' present at the thermometer code generated by a fast flash A/D-converter are removed. For this correction operation simulations are given.

WPA14-24 -- A Fuzzy reasoning based approach for ARMA order selection

Haseyama, Miki; Emura, Masafumi; and Kitajma, Hideo, *Hokkaido University*

A fuzzy reasoning based approach for ARMA order selection is discussed in this paper. The proposed method attempts to select the optimal ARMA order of a time-varying ARMA model. This method improves model validity-criterion based order selection, such as the AIC (Akaike's Information Criterion) and the MDL (Minimum Description Length), etc., with applying both fuzzy reasoning and fuzzy c-means clustering methods. These fuzzy methods are incorporated in the proposed method as follows: (1) Suppose the ARMA order of the reference time-varying model changes. The suitable ARMA order is selected by utilizing the recursive fuzzy reasoning method. (2) By using the fuzzy c-means clustering method, we detect the time at which the ARMA order of the reference model changes, and the clustering values are used for adaptively setting the forgetting factor in the recursive fuzzy reasoning method.

WPA15 – Analog Circuits and Systems — Poster Session

Chair: Todd R. Weatherford

Naval Postgraduate School

2:00pm – 5:30pm - ***Room: Serra Ballroom - Back III***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPA15-1 -- 7 Gbit/s Measurements on a 0.8 um CMOS Line-Receiver

Johansson, Henrik O., *Linköping University*

Successful sampling of every 32nd bit in a 7-Gbit/s data stream has been shown with a 0.8-um CMOS circuit which is based on parallel sampling. The input bandwidth of the chip is the suspected bit rate limiting factor. The input bandwidth is mainly set by the wire characteristic impedance and the input capacitance of the chip. Half of a 5-Gbit/s data stream has been received by the same circuit. This indicates that (full) reception of 5-Gbit/s data-streams is possible. The bit rate limiting factor in this case is the accuracy and jitter of the control-clocks to the sampling-switches.

WPA15-2 -- AlGaAs/GaAs HEMT 5-12 GHz Integrated System for an Optical Receiver

Reina, Rodrigo and Olmos, Alfredo, *Universidade de Sao Paulo* and Charry, Edgar, *CPqD - Telebras*

We report the design of a chip-set containing several key components for an optical receiver in GaAs/AlGaAs HEMT technology. Different building blocks necessary to regenerate the signal coming from an optical data link have been characterized. The system provides a -3dB bandwidth of 5 Ghz with a transimpedance of 2.4 KOhms. Power consumption was estimated to be 350 mW at that frequency. Current ranging from 20 mA to 300 mA, might be processed with this receiver. This current range was achieved with an AGC control unit. An appropriate output buffer allows matching to a 50 Ohms measurement equipment. The dynamic range is of 12.2 dB. Circuit was fabricated at external foundry.

WPA15-3 -- Multiple 1:N Interpolation FIR Filter Design Based on a Single Architecture

Kang, In and Yeon, Kwang-Il, *Electronics and Telecommunications Research Institute (ETRI)*, Jo, Han-Cheol, *Doowon Technical College*, Chong, Jong-Hwa, *HanYang University* and Kim, Kyungsoo, *Electronics and Telecommunications Research Institute (ETRI)*

A VLSI architecture for multiple 1:N interpolation FIR filter is proposed for QPSK modulation in WLL. Multiple filters are operated synchronously and N outputs are generated in case of 1:N interpolation. But the architecture and the operating frequency are the same as those of single FIR filter architecture except having pipeline registers. Because of using a single architecture, proposed architecture can be implemented with less chip area. The power consumption is not increased because its operating frequency is the same as that of single architecture. When N is 4, four-output 1:4 interpolation filter is designed using VHDL logic synthesis. The number of gates and operating frequency are compared with those of transversal FIR filter design method and look-up table design method.

WPA15-4 -- VLSI Architectures for Weighted Order Statistic (WOS) Filters

Chakraharti, Chaitali, *Arizona State University*; and Lucke, Lori E., *Minnetronix, Inc.*

The class of median filters has been extended to include weighted order statistics (WOS) filters, to improve the flexibility of the filtering operation. The WOS filter weights each input within a sample window, and thus retains the original temporal information. In this paper, we present efficient VLSI architectures for nonrecursive and recursive WOS filters based on (i) array, (ii) stack filter, and (iii) sorting network structures. All these architectures maintain a weighted rank for each sample in the sample window. As the window shifts for each new output, the weighted ranks are updated. We analyze the implementation complexity for each architecture and verify our results through physical implementations.

WPA15-5 -- Analog CMOS Design of the Incremental Credit Assignment (ICRA) Scheme for Time

Series Classification

Vlassis, S.; Siskos, S.; Hatzopoulos, Alkiviades A., Petrides, Kehapious V.; and Kehagias, A., *Aristotle University of Thessaloniki*

The Incremental CRedit Assignment (ICRA) scheme has been introduced in [1] and its application to time series classification has been shown by simulation results. In this work an analog CMOS design of its decision module is described and its characteristics are given. The performance of the analog CMOS circuit was according to the theoretical simulations and the results obtained were very promising for the application of the circuit in practical classification problems, like speech recognition.

WPA15-6 -- MOSFET Stair-Shaped I-V Circuit and Applications

Jun, Sibum, *LG Semicon Co., Ltd.* and Ahn, Su Jin, *POSTECH*

A new circuit block having a stair-shaped I-V curve is described. The proposed circuit is based on novel configuration of three cascode branchs. Furthermore, 4-level quantizing inverter and 4-level latch utilizing the proposed circuit are also presented. Unlike the previous work, these works are compatible with a standard CMOS technology.

WPA15-7 -- Statistical Design Techniques for Yield Enhancement of Low Voltage CMOS VLSI

Tarim, Tuna B. and Kuntman, H. Hakan, *Istanbul Technical University;* and Ismail, Mohammed, *Ohio State University*

Since random device/process variations do not scale down with feature size or supply voltage, statistical design of low voltage circuits is essential in order to keep functional yields of low voltage circuits at levels that are competitive and cost effective. This is particularly true for low voltage analog ICs. This paper presents a robust design of a low voltage square-law CMOS composite cell, using statistical VLSI design tools. The Response Surface Methodology and Design of Experiment techniques were used as statistical tools. This paper shows that statistical techniques will result in area/layout optimization which will enhance functional yield of low voltage analog ICs.

WPA15-8 -- A Novel Digitally Controlled CMOS Current Follower for Low Voltage Low Power Applications

Elwan, Hassan O. and Ismail, Mohammed, *Ohio State University*

In this paper fully differential digitally controlled analog library cells are given. The proposed cells are based on a novel digitally controlled current follower (DCCF) circuit. The proposed circuits are useful for low voltage low power high frequency applications. The DCCF operates from a 3V supply in class AB mode and provides a bandwidth of 80MHz in 1.2mm CMOS technology. Owing to the class AB operation of the DCCF circuit the standby current is below 94mA. The proposed circuit is used to realize digitally controlled weighted sum transconductors and MOSFET-C filters. APLAC simulations based on the AMI 1.2mm n-well level 3 parameters are in agreement with the presented work
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WPA15-9 -- An Analytical Solution for a Class of Oscillators and its Application to Filter Tunning

Pavan, Shanthi, *Texas Instruments, New Jersey* and Tsividis, Yannis, *Columbia University*

We present a completely analytical solution to a filter comparator oscillator system and verify it by macro-model simulations and experiment. We discuss the applications of this kind of oscillator in a vector-locked loop system for continuous time filter tuning.

WPA15-11 -- Active Capacitance Multipliers Using Current Conveyors

Di Cataldo, G., *Universita di Catania*; Ferri, G., *Universita Di L'Aquila*; and Pennisi, Salvatore, *Università di Catania*

One of the most limiting problems in the design of integrated circuits is constituted by the realization of high valued capacitors, who have the heavy drawback of high occupation of silicon area. Moreover, in some sensor applications, it can be useful to deal with capacitance values higher than those normally given by capacitive sensors. In these cases, the use of capacitance multipliers can be very important. In this paper, we propose a novel principle of simple capacitance multipliers, by which it is possible to obtain higher capacitive values. Two solutions, the first using one CCII- with current gain and the second using two conventional CCIIs, are presented and analyzed. The effects of CCII non-idealities are also evaluated and discussed. Finally, SPICE simulations, which are in a close agreement with the analytical calculations, are also reported.

WPA15-12 -- A +\-1.5V CMOS Four-Quadrant Analogue Multiplier Using 3GHz Analogue Squaring Circuits

Di Cataldo, G., *Universita di Catania*; Ferri, G., *Universita Di L'Aquila*; and Pennisi, Salvatore, *Università di Catania*

A CMOS four-quadrant analog multiplier using the MOS transistors operated in triode region is proposed. The multiplier is basically constructed by voltage substractors for two differential inputs, and two 3GHz analog squarers for multiplication. Simulation results are given to verify the theoretical analysis. the multiplier has a nonlinearity error less than 1% over ±1.5V input range. The circuit provides a -3dB

bandwidth higher than 1.2GHz and exhibits a THD lower than 4% with a 1.5V peak-to-peak input voltage, which dissipating 249mW. The second-order effects including mismatch effects are discussed The proposed circuit will be useful in analog RF signal-processing applications.

WPA15-13 -- An Autozeroing Floating-Gate Second-Order Filter

Hasler, Paul, *Georgia Institute of Technology;* Stanford, Theron, *California Institute of Technology;* Minch, Bradley A., *Cornell University;* and Diorio, Chris, *University of Washington*

We introduce the Autozeroing Floating-Gate Second-Order Section. We built this second-order filter where the corner frequency and Q are electronically tunable based on a classic filter topology and principles of OTA amplifiers. We built this second-order filter using three AFGAs---our floating-gate amplifier that sets its operating point adaptively by the interaction of hot-electron--injection and electron-tunneling currents.

WPA15-14 -- Design of Equalizer Using Phase Delay Characteristic

Carvalho, Delmar B., *Federal University of Santa Catarina/Caikelic University of Peletas*; Filho, Sidnei Noceti, *LINSE/EEL/CTC/UFSC*, Seara, Rui, *Federal University of Santa Catarina*

This paper proposes a new approach via phase delay as an advantageous alternative with respect to group delay for phase equalization. This procedure presents, as a main advantage, the absence of phase-intercept distortion.

WPA15-16 -- New Switched-Current Circuits for Nonlinear Signal Processing

Zeng, X. and Tang, P.S., *Fudan University;* and Tse, C. K., *Hong Kong Polytechnic University*

The application of switched-current techniques for nonlinear sampled-data signal processing is a new application area compared with the switched-current frequency domain linear filtering applications. This paper proposes several new switched-current circuits for nonlinear signal processing. These are switched-current pulse-width modulator, switched-current current-controlled oscillator and switched-current multiplier-divider. The proposed circuits present merits of simple circuit configuration, low voltage and low fabrication cost.

WPA15-17 -- A Replica Bising for Constant-Gain CMOS Open-Loop Amplifiers

Palmisano, Giuseppe and Salerno, R., *Università di Catania*

A replica biasing circuit is proposed which allows open-loop gain in CMOS amplifiers to be accurately set. The approach can be applied to both RF and IF amplifiers whereas resistive loads have to be employed to achieve high frequency and low noise performance. The simulated results show a sensitivity to process tolerances and temperature variations which is lower than that of traditional approaches.

WPA15-18 -- Switched-Capacitor Impedance Simulation Circuits Realized with Current Conveyor

Ono, Toshio, *Saitama Institute of Technology*

This paper describes switched-capacitor (SC) inductor and Frequency Dependent Negative Resistor (FDNR) which use second generation Current Conveyor (CC II). In general CC II's used in SC circuits are not always used as CC II and there are phase periods in which CC II behaves as much simpler active device like unity gain buffer (UGB). In this paper, CC II's in SC circuits always behave as CC II to make full use of CC II. Then SC inductor in which effects of parasitic capacitors can be easily reduced is proposed. And SC FDNR which uses CC II to get a simple circuit structure is also proposed. Both circuits are controlled by simple 2 phase control clock. The spreads of capacitor values are 1. the sum of capacitor values of SC FDNR is 4. This value is the smallest value in SC FDNR circuits reported already. Simulation results by SWITCAP and experimental results by discrete components are shown.

WPA15-19 -- A Simple CMOS Digital Controlled Oscillator with High Resolution and Linearity

To, Cheuk-Him; Chan, Cheong-Fat; and Choy, Oliver Chiu-Sing, *The Chinese University of Hong Kong*

This paper presents a new DCO (digital controlled oscillator) circuit which has a very simple structure with high resolution and linearity. For example, a six bit DCO only requires seventeen MOS transistors. As a result of the simple structure, the new DCO also consumes less power compared to other DCO designs. Another added feature of this new design is that the output signal can be phase-locked to an external input signal. A four bit DCO test circuit was fabricated with a 0.7 micron CMOS technology. The test circuit has a die size of 0.024 sq. mm and an operating frequency range from 13MHz to 50MHz.

WPA15-20 -- On Optimizing Micropower MOS Regulated Cascode Circuits on Switched Current Techniques

De Lima, Jader Alves, *Universidade Estadual Paulista*

Trade-off between settling time and micropower consumption in MOS regulated cascode current sources as building parts in high-accuracy, current-switching D/A converters is analyzed. The regulation-loop frequency characteristic is obtained and difficulties to impose a dominant-pole condition to the resulting 2nd-order system are discussed. Raising pole frequencies while meeting consumption requirements is basically limited by parasitic capacitances. An alternative is found by imposing a twin-pole system in which design constraints are somewhat relaxed and settling slightly faster. Relationships between pole frequencies, transistor geometry and bias are established. Simulated waveforms obtained with PSpice of designed circuits following a voltage perturbation suggest a good agreement with theory. The proposed approach applied to the design of a micropower current-mode D/A converter improves its simulated settling performance.

WPA15-21 -- Elimination of Nonlinear Clock Feedthrough in Component-Simulation Switched-

Current Circuits

de Queiroz, Antonio Carlos M. and Schechtman, Jones, *Universidade Federal do Rio de Janeiro*

This paper discusses a technique for the cancellation of clock feedthrough effects in component-simulation switched-current filters, based on a scaled replication of the parts of the circuit that control the filter coefficients. The regular structure of these filters is particularly convenient for the application of the technique, that can also be applied to other structures. As additional benefit, considerable layout simplification can be obtained, because the same technique cancels systematic errors in transistor widths, what allows layouts to be done without splitting the coefficient-controlling transistors in several identical units, as usually done for better matching.

WPA15-22 -- Analog Building Blocks for a Sampled Data Fast Wavelet Transform CMOS VLSI Implementation

Gonzalez-Altamir, Gerardo and Ramirez-Angulo, Jaime, *New Mexico State University*

A set of high performance analog blocks, used for a sampled data fast wavelet transform chip, is presented. Use of novel techniques based on Multiple-Input Floating-Gate MOS transistors enhances the circuits characteristics. Control circuits using these devices allow to improve behavior parameters such as bandwidth, distortion, common-mode, and unity-gain compensation. An improved voltage follower circuit using these blocks is discussed. Simulations results are presented.

WPA15-23 -- An Area Efficient Time-Interleaved Parallel Delta-Sigma A/D Converter

Eshraghi, Aria and Fiez, Terri, *Washington State University*

Using a time-interleaved A/D converter is one method of obtaining a Nyquist-rate A/D converter from delta-sigma A/D converters. In this paper, it is shown that the performance of the time-interleaved delta-sigma A/D converter is as good as other forms of parallel delta-sigma A/D converters. The issue associated with the gain mismatch among the channels is addressed with a proposed solution to circumvent the channel matching problem.

WPA15-24 -- Program Delivery Control with On-Screen Display

Peng, Dennis Lee Chew; Cheung, Chu Ming; Liang, Joseph; and Yong, Teo Tee, *Siemens Components Pte Ltd.*

This paper presents a teletext decoder IC that receives all VPS, 8/30 format 1 and 2 and teletext header data. It is integrated with an On-Screen Display function that can be synchronise to a CVBS signal or generate a complete multi-standard (PAL/NTSC) CVBS signal with a full screen colored OSD.

WPB4 – Field Programmable Gate Arrays
Chair: Sachin Sapatnekar
University of Minnesota

4:00pm – 5:30pm - ***Room: Ferrante I***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPB4-1 -- Using PLAs to design Universal Logic Modules in FPGAs

Lee, Kok Kiong and Wong, Martin D. F., *The University of Texas at Austin*

We consider implementing Universal Logic Modules in Field Programmable Gate Arrays (FPGAs) with Programmable Logic Arrays (PLAs) using a reduced number of programmable switches. These have the advantages of a regular structure and are very easy to program. By suitably reducing the number of switches in a PLA, the total number of switches is reduced tremendously, while the PLA still remains functionally complete. Since switch features take up more space than other logic elements, the savings can translate to a reduction in area. The reduction in programmable switches implies that a smaller number of programming bits is required for each ULM. We obtained 3-input and 4-input ULMs using 5 and 13 programmable switches respectively, matching previous results but in a smaller area. Technology mapping is also very simple. We also obtain approximate ULMs with very high coverage. We obtained an approximate ULM using 11 programming switches which covers 99% of all 4-input functions, using a much smaller area than a previous result.

WPB4-2 -- FPGA Maping of Sequential Circuits with Retiming

Lee, Jun-yong, *Hongik University*

Constructive and iterative steps of FPGA mapping algorithms for sequential circuits are enhanced by retiming technique and fuzzy logic.Multiple criteria measured for design data are connected by a hierarchical structure of fuzzy logic rules for decision making.The discussed mapper outperforms commercial tools in both area and timing for substantial set of MCNC benchmarks.

WPB4-3 -- RAISE: A Detailed Routing Algorithm for SRAM Based Field-Programmable Gate Arrays Using Multiplexed Switches

Baena, Vicente; Aguirre, Miguel Angel, and Torralba, Antonio, *ESI-(Grupo de Tecnologia Electronica);* and Faura, Julio, *Sidsa*

This paper describes a new detailed routing algorithm, specially designed for those architectures that are found in most recent generations of Field-Programmable Gate Arrays (FPGAs). The algorithm also brings a solution for those architectures where multiplexed switches are used in order to decrease the chip area like the recently proposed FIPSOC FPGA. The algorithm, called RAISE, can be applied to a broad range of optimizations problems and has been used for detailed routing of symmetrical FPGAs, whose routing architecture consists of rows and columns of logic cells interconnected by routing channels, with or without the use of multiplexed switches. RAISE (Router using AdaptIve Simulated Evolution) searches not just for a possible solution, but tries to find the one with minimum delay. Excellent routing results have been obtained over a set of several benchmark circuits getting solutions close to the minimum number of tracks.

WPB4-4 -- Rapid Prototype of a Fast Data Encryption Standard With Integrity Processing for Cryptographic Applications

Guendouz, Hassina, *Ecole Centrale Electronique*; and Bouaziz, Samir, *Universite Paris*

In this paper we present the design of a chip for real-time cryptographic processing in industrial applications. The chip acts as a co-processor of a system for the automatic ciphering and data integrity processing : it implements the DES/MAC algorithm (Data Encryption Standard/Message Authentication Code) in the same silicon area with high speed performance. These research come within a process aiming at reaching an implementation onto specialised pipeline and parallel architecture from algorithm specification.The design has been performed in rapid prototype ACTEL Programmable Gate Array Device using an approach based on high level transformations on the VHDL specifications. This paper is in part of an European Program which aims to design a macro cell library for cryptographic applications

WPB13 – Circuits and Systems for Communication Networks II Poster Session

Co-Chair: Joseph Kahn
University of California
Co-Chair: Chung-Sheng Li
IBM

2:00pm – 5:30pm - ***Room: Serra Ballroom – Back !***

*3:30 pm –4:00pm – Coffee Break in **DeAnza Ballroom** with Exhibitors*

WPB13-1 -- Compile-Time Priority Assignment and Re-routing for Communication Minimization in Parallel Systems

Sha, Edwin; Surma, David R., and Kogge, Peter M., *University of Notre Dame*

The performance gains of massively parallel systems can be significantly diminished by the inherent communication overhead. This overhead is caused by the required message passing resulting from the task allocation scheme. To minimize this overhead, a hybrid static-dynamic scheduling technique is presented. The static phase makes use of a priori information at compile-time to assign priorities to each message transmission. The priorities are determined using the recently developed Collision Graph model and are utilized at run-time to arbitrate the message transmissions. Determining an optimal priority scheme is an NP-Complete problem. Therefore the developed techniques employ heuristics and a flexible routing scheme to deal with a general case model of message traffic. Experiments performed show a significant improvement over baseline approaches.

WPB13-2 -- A VLSI Design of Dual-Loop Automatic Gain Control for Dual-Mode QAM/VSB

Wang, Chorng-kuang; Shiue, Muh-Tian; Huang, Kuang-Hu, and Lu, Cheng-Chang, *National Central University*; and Way, Winston I., *National Chiao Tung University*

A digitized automatic gain control (DAGC) whose loop bandwidth can be automatically regulated by a digital quantizer is presented in this paper. The designed quantizer that only costs tens of gates provides the DAGC both wide loop bandwidth for fast acquisition and narrow loop bandwidth for low AGC gain jitter in stable steady-state. The receive bandpass filter, variable gain amplifier (VGA), and digital control circuits gave been implemented in VLSI using 0.8mm CMOS technology. For both 64-QAM and 8-VSB signals, the closed-loop experimental results show that the designed DAGC has input dynamic range from 22mBpp to 456mVpp, transient mode bandwidth 1kHz, steady-state bandwidth 90Hz, settling time of step response less than 2ms using 10MHz clock for digital control chip.

WPB13-3 -- Routing Multipoint Connections in Computer Networks

Wensheng, Sun, *Beijing University of Posts and Telecommunications*

This paper studies the problem of constructing minimum-cost multicast trees with end-to-end delay and delay variation constraints to meet the quality of service (QoS) requirements of real-time interactive applications operated in high-speed packet-switched environments. The paper first discusses the routing problem with bounded delay along the paths from the source to each destination and bounded variation among the delays along these paths, and then presents a new algorithm based on Hopfield neural networks to optimize the multicast tree with delay and delay variation constraints. The simulations show that the proposed algorithm achieves its best performance in constructing constrained multicast tree in computer networks.

WPB13-4 -- Dynamic Routing Algorithms in ATM Networks

Feng, Gang, *Beijing University. of Posts &Telecom.*

In our previous work, we elaborated the multistage virtual path(VP) control strategy and the VP topology optimization problem in which we assume a set of alternative routes exist between each source-destination (SD) pair. In the first part of this paper, a supplementary algorithm, which can yield all possible routes between two nodes and can be used for general routing problems, is provided. Based this algorithm, a dynamic VC routing policy is studied. The proposed policy distinguishes from other strategies in that it is considered in a generic networking environment. In the last part of this paper, we present a dynamic VP routing algorithm which is an important component of the dynamic VC routing policy. Detailed analyses and experimental results demonstrate these algorithms are correct, practical and useful.

WPB13-5 -- A New Memory Controller for the Shared Multibuffer ATM Switch with Multicast Functions

Chang, Robert Chen-hao, *National Chung-Hsing Univ.*

A novel ATM switch memory controller incorporated the shared multibuffer architecture is proposed. By applying the cyclic N method at the address queues, the blocking effect is eliminated and no memory and cross-point switch speed up is required. Multicast functions are efficiently carried out via a multicast queue. Each multicast packet only occupies one space in buffer memory and no additional copy circuit or counter is needed. Thus, the buffer utilization is improved and the hardware complexity is reduced. With the aid of the input traffic adaptive controller, multicast packets are dynamically sent to the output ports according to the input traffic patterns so that the unfairness problem due to employing the multicast queue is alleviated. By adopting the new memory controller, the throughput can be elevated to about 99.2%.

WPB13-6 -- Scheduling Algorithm for Real-time Burst Traffic using Dynamic Weighted Round Robin

Kwon, Taeck-Geun; Lee, Sook-Hyang; Rho, June-Kyung, and Kwon, Taeck-Geun, *LG Information & Communications, Ltd.*

In this paper, we propose a new scheduling algorithm, called the Dynamic Weighted Round Robin (DWRR) scheduling discipline, which is suitable for real-time variable bit rate (rtVBR) service as well as other services such as constant bit rate (CBR), non real-time VBR (nrtVBR), available bit rate (ABR) services in a high-speed network. We employ dynamic weight to serve a queue associated with active and busy connection with strict delay and bandwidth requirements. This adaptive scheduling algorithm enables a network to provide multimedia service characterized by integrated and burst traffic.We finally compare our new algorithm with existing one in terms of fairness and Quality of Service (QoS) guarantee by simulation study.

WPB13-7 -- Design and Implementation of an ATM Segmentation Engine with PCI Interface

Kim, Chan; Jun, Jong Arm; Lee, Kyou Ho, and Kim, Hyup Jong, *Electronics and Telecommuncations Research Institute*

This paper describes the design and implementation of an ATM Segmentation Engine including PCI interface. This engine, which was designed for an ASIC called ASAH-NIC, contains DMA read machine and segmen-tation machine. It uses local memory where control in-formation is stored in schedule table, VC table, buffer descriptor and status queue. It has several spepcial fea-tures like processing split packet buffers and automatic alignment and packing of transmit data.

WPB13-8 -- A Novel Neural Estimator for Call Admission Control and Buffer Design in ATM Network

Zhang, Liang and Liu, Zemin, *Beijing University of Posts & Telecommunications*

In call admission control of ATM network, it is difficult for the conventional method to judge the accepting boundary accurately and dynamically, for the imprecision description of the traffic parameters and the different requirement of the allowed QoS. In this paper we propose a novel neural network structure as an intelligent control scheme to perform ATM admission control. The neural estimator can learn the probability distribution of the CLR, thus can control the ATM traffic very accurately and dynamically. The disperse structure of the neural estimator make it easy to learn and operate. The trained neural network can also be used as a buffer estimator in the reference design of ATM system. The simulation result show the advantage of this neural estimator.

WPB13-9 -- DCT Based Error Concealment for RTSP Video over a Modem Internet Connection

Chung,Yon Jun,*University of Southern California*

Data lost in the form of dropped packets is a major obstacle to actualizing real time Internet video via modem connection with frame rates as high as 30 frames per second. Error concealment (EC) techniques must restore the lost data. Due to rigid system specifications of this application, only the computationally simplest error concealment methods are plausible. Replication, which is the simplest temporal error concealment (TEC) method, fits well in this situation. There are however circumstances when replication is inadequate and linear

interpolation, the simplest spatial EC, is used in its place. In this work, we consider an alternative spatial EC to linear interpolation, i.e. the DCT-coefficient based EC algorithm, with comparable computational cost and consistently better image quality in real-time Internet video applications.

WPB13-10 -- A Transmitting and Receiving Method for CDMA Communications Over Indoor Electrical power Lines

Okazaki, Hideaki, *Gifu National College of Tech.*; and Kawashima, Mitsusato, *Ibiden Industries Co.,LTD*

Transmitting and receiving method for CDMA communications through 2-wire or 3-wire power line cord over indoor power lines are proposed. The key idea for transmitting method is to use a fundamental model of a coupling transformer-less transmitting circuit including the influence of the distribution transformer and to find out the combinations of model parameters giving the acceptable distortion of the transmitted waveforms for CDMA communications. That for receiving method is to use a filtering method that separates arbitrary waveforms of transmitted data signal from the superposition waveforms of the sinusoidal high power signal and transmitted data signal without distorting arbitrary waveforms of transmitting signal at all. These methods are experimentally confirmed to be effective.

WPB13-11 -- Network Design and Control for Multipoint-to-Multipoint Communications

Kinoshita, Kazuhiko, *Osaka University*; Soeda, Junichiro, *Matsushita Electric Industrial Co.,LTD*; Yamai, Nariyoshi; Takine, Tetsuya; and Murakami, Koso, *Osaka University*

This paper considers the network design and control for multipoint-to-multipoint communications. We propose a new routing control method which includes the member connection method and the route setup algorithm. The former implies that each member has its own route to send information to other members. Thus it can avoid traffic concentration in a particular route. Further, in the route setup algorithm, all routes are generated in parallel, by adding a link, which have lower-cost and lower-load, one by one, based on grouping by the number of destination nodes on the route. An interesting feature of the proposed algorithm is that every route can be established with a unified algorithm, even when newcomers join ongoing communications. In addition to the above method, we also propose a network design algorithm. It can make the proposed routing control method more effective. Simulation experiments show that the proposed framework is suitable for multipoint-to-multipoint communications.

WPB13 -- 12 A Multi-Rate Channelized Wireless LAN System with Fixed Channel Assignment

Ko, Tsz-Mei and Lam, Chi-Wai, *Hong Kong Univ of Sci and Tech*

We consider a multi-rate channelized wireless LAN system for a typical office building. The problem is formulated as a fixed channel assignment problem with multi-rate traffic. We generalized several known fixed channel assignment algorithms which were originally designed for single rate cellular networks. A new lower bound called the generalized clique bound is obtained. The generalized algorithms are compared via simulations for several typical office environments. It is found that these algorithms perform almost optimally, i.e., use the least bandwidth to satisfy the call requirements, when compared with the generalized clique bound.

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